

Low Power Radiation Tolerant VLSI for Advanced Spacecraft

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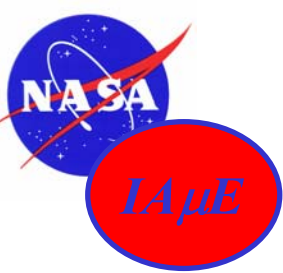
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Overview

Introduction

Ultra-Low-Power CMOS

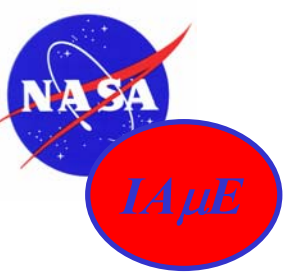
Radiation-Tolerant VLSI

Radiation-Tolerant Ultra Low Power

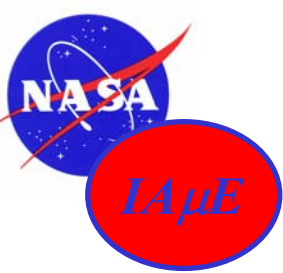
ULP-3 Chips

Ultra Low Power NASA Missions

Conclusions



Ultra-Low-Power CMOS



CMOS Power Consumption

$$P_{TOTAL} = P_{DC} + P_{AC}$$

$$P_{DC} = \text{Leakage}$$

$$P_{DC} = V_{SUPPLY} \times I_{LEAK}$$

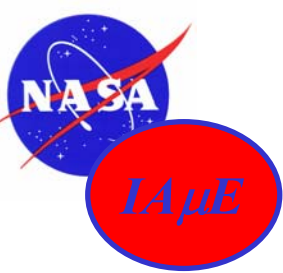
$$P_{AC} = \text{Switching power}$$

$$P_{AC} = V_{SUPPLY}^2 \times F_{CLOCK}$$

For circuits with low activity, P_{DC} dominates.

For circuits with high activity, P_{AC} dominates.

The most effective way to reduce power consumption in active circuits is to reduce the supply voltage. We seek a balance between dynamic and static power consumption.



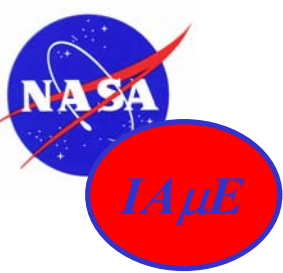
$\frac{1}{2}V$ Supply Operation

ULP Process reduces V_{DD} from 3.3V to 500 mV

- Standard AMI 0.35 μ process with one additional implant.
- Normally, we design process for threshold $V_T=100\text{mV}$ to 170mV

Required for performance & noise immunity

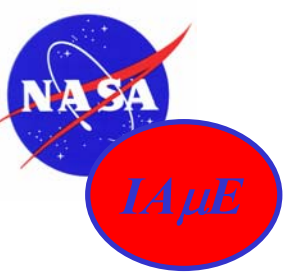
- Difficult to maintain V_T in this range with process alone:
 1. Process variation
 2. Temperature



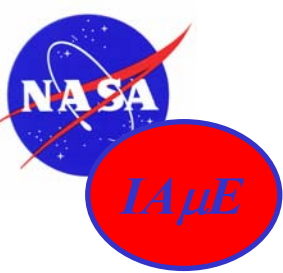
Active Threshold Control

Use Active Threshold Control to Adjust V_T

- Design process for $V_T \approx 0$
- Adjust back bias (V_{SB}) to set desired threshold.
- Electronically stabilized V_T operates safely in 100-170 mV range.
- Area penalty $< 15\%$.
- Back bias becomes a design parameter.

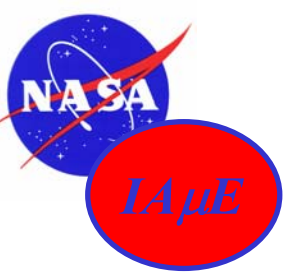


Radiation Tolerant CMOS



Radiation Tolerant vs Radiation Hard

Radiation Effect	Radiation Tolerant	Radiation Hard
Total Ionizing Dose (rad (Si))	>50K	1Meg
SEU LET (MeV-cm ² /mg)	>40	>40
SEL LET (MeV-cm ² /mg)	>120	>120



Radiation Tolerant CMOS from Commerical Foundaries

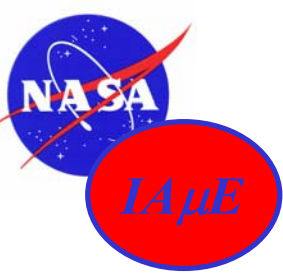
Advantages

Significant cost savings.

Enables new designs to track process improvements.

Enables use of existing intellectual property (macrocells, cores).

When incorporated into standard cells, radiation tolerant technologies enable use of commercial synthesis and place and route tools, with significant enhancement of the design process.



Single Event Upset (SEU)

Problem

Strike by a charged ion introduces electron-hole pairs.
Can cause a memory element to change state.

Mitigation

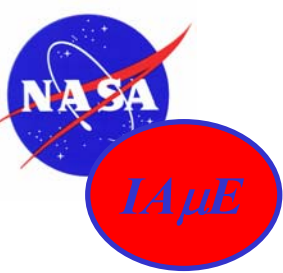
12-transistor, self-correcting memory element.
Feedback circuit detects change of state and reverses it.

Cost

$\approx 1.6 \times$ Increase in area, in standard cell implementation.
Some increase in power consumption.

Advantages Over Some Other Approaches

Reduced power consumption, improved switching speed
compared to resistive approaches.



Single Event Latchup

Problem

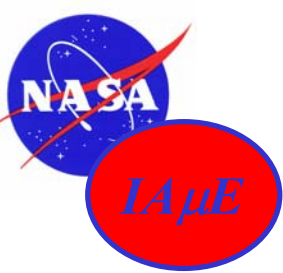
Charged particle penetrates chip, creates electron-hole pairs.
Can initiate positive feedback in parasitic transistors
Induces latchup.

Mitigation

Guard bands drain off charge, prevent latchup..

Cost

Increased area for guard bands.
Area cost significantly reduced, when guard bands overlie
ULP body ties.



Total Ionizing Dose

Problem

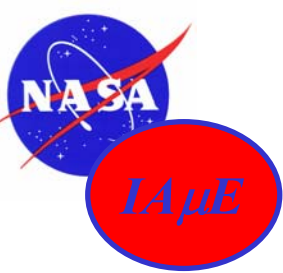
Charged particles trapped in oxide.
Lowers threshold of nMOS transistors.
Raises threshold of pMOS transistors.

Gate Oxide: low risk

High gate oxide discourages entrapment of particles.
Thin gate oxide, particles anneal out easily.

Field Oxide: high risk

Low oxide purity oxide encourages entrapment of particles.
Thick oxide, particles anneal out slowly.
Lowers threshold of n-type parasitic transistors.
Increases parasitic leakage, eventually affects operation.



Radiation Tolerant-Ultra Low Power

Total Ionizing Dose

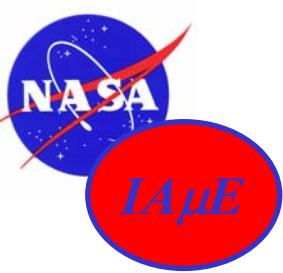
- ULP Back Bias Improves TID Resistant
- Raises the threshold of parasitic nMOS transistors.
- Parasitic pMOS transistor thresholds already high.
- Reduces leakage and circuit failures due to TID.

Single Event Latchup

Low-voltage devices inherently latchup-resistant.
Insufficient voltage to initiate latchup.

Single Event Upset

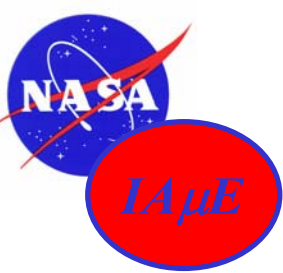
Low-voltage devices more susceptible to SEU.
SEU mitigation techniques improve SEU resistance.



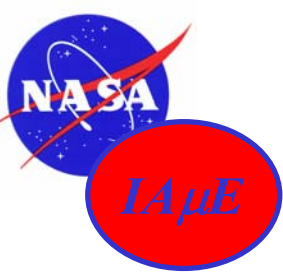
ULP-3 Chips

Name	Function	Features	Speed
RS16e	RS Encoder	Non-RT CCSDS, T=16	320 Mbits/sec
RS16es	RS Encoder	RT CCSDS, T=16	320 Mbits/sec
RS5d	RS Decoder	Non-RT EDACS, T=5	1 Gbit/sec
Quad RS8	Quad RS Decoder	Non-RT T=8	680 Mbits/sec
USESs	Data Compression	RT USES	40 MHz
C8051s	Microcontroller	RT 80C51	25 MHz
C50	DSP	Non-RT (Navy)	25 MHz

These chips have been fabricated, and are currently being tested.



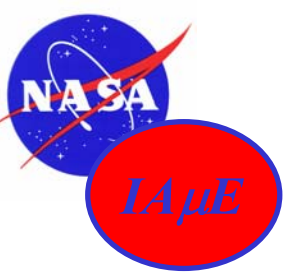
Test Results



Power Comparison

Freq (MHz)	3.3V Encoder		0.5V Encoder		Power Reduction Factor
	Total Power (mW)	Static Power (mW)	Total Power (mW)	Static Power (mW)	
1.0	28.48	0.00	2.25	2.17	12.70
5.0	54.78	0.00	2.68	2.16	20.40
10.0	83.66	0.00	3.19	2.15	26.20
20.0	150.18	0.00	4.15	2.15	36.20

Non-SEU-immune Reed-Solomon Encoders.
Back bias = 3.0V



Power Comments

As expected, dynamic power saving improves with clock frequency

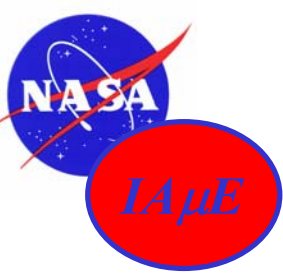
At 20 MHZ:

Dynamic power = Static power

Optimal operating condition

Theoretical limit on dynamic
power savings factor:

$$\left(\frac{3.3}{0.5}\right)^2 = 43.6$$



Total Dose Tests

Total dose testing at Naval Research Labs

- Up to 200 KRad/Si
- 8 kV copper x-rays @ 50 rad(Si)/sec
- nMOS devices biased “on” or “off”

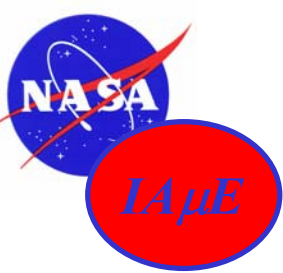
0.5V and 3.3V Devices: Back bias = 0V

0.5V devices has 4 orders of magnitude less radiation-induced leakage than 3.3V devices.

0.5V Devices: Back bias = 2V

No significant difference between pre- and post-irradiation curves; no detectable degradation up to 200 KRad/Si.

GSFC duplicated results; also tested ULP CCSDS Reed Solomon encoder at 200 KRad(Si) with no significant degradation.



Single Event Effects Testing

ULP-2 Chips tested at the Twin Tandem Van de Graff Facility, Brookhaven National Laboratory.

Test Structures

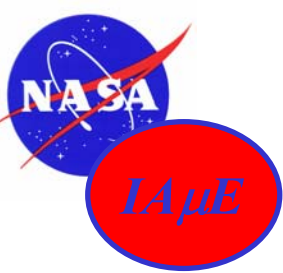
32-bit shift registers

Shift registers made from different flip flop types:

1. Prototype SEU flip flops
2. Standard, non-radiation-tolerant flip flops

Each FF: one global clock phase; 2nd phase generated internally

- Both 3.3V and 0.5V parts tested
- 0.5V parts tested with range of back bias settings: 0-2V



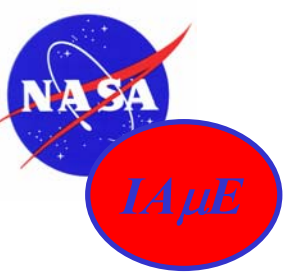
SEE Test Summary

Single Event Upset

- As expected, low-voltage devices more susceptible to SEU
- Prototype SEU flip flops less susceptible than non-RT
- First upsets at 10 MeV/mg/cm^2
- Several opportunities for improvement have been found
- Improved SEU flop flops have been designed and schedule for fabrication and testing.

Single Event Latchup

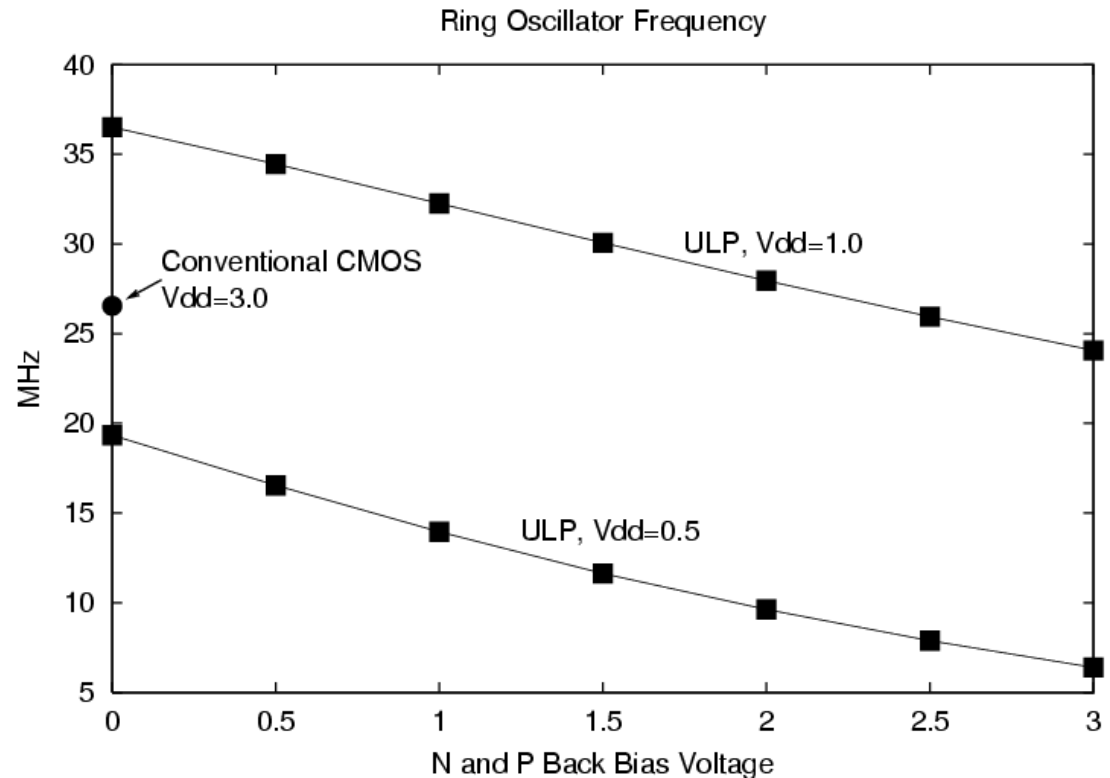
ULP Circuits experienced no latchup.



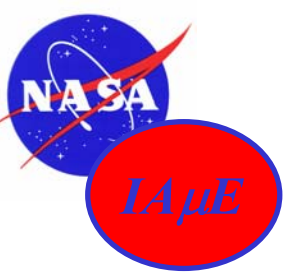
Back Bias and Performance

Note

1. nMOS and pMOS transistors have same back bias.
2. Studies are underway to determine optimal, individual back bias.



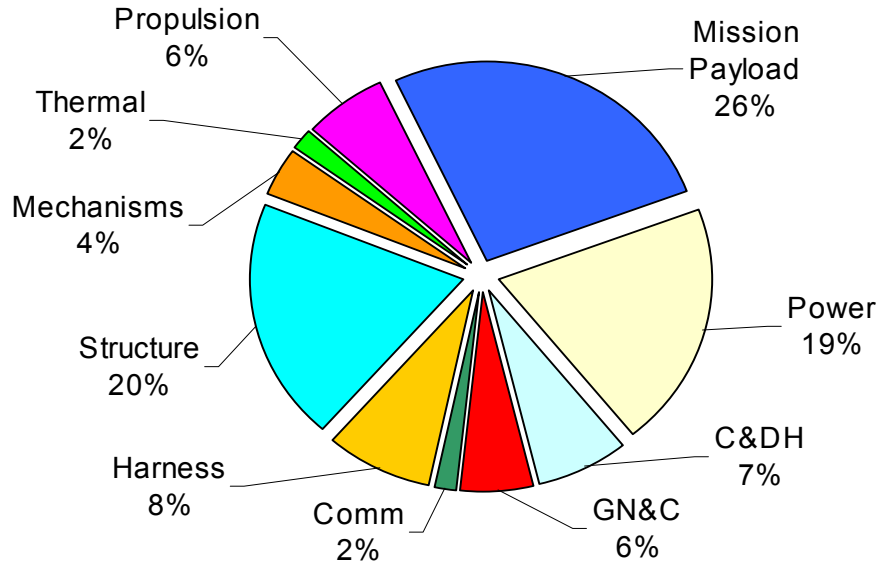
By trading off back bias for performance, we can dynamically adjust power consumption according to mission needs.



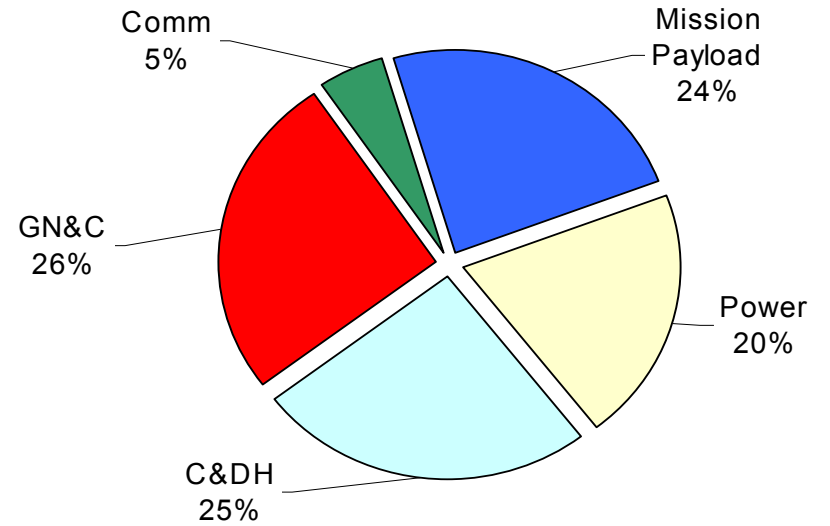
Planned Ultra Low Power NASA Missions

Mission	Description	Center	ULP Device
NMP E03	GIFTS- IOMI	LaRC	Microcontroller RS16 Encoder USES
NMP ST5	Microsat/ Nanosat	GSFC	RS16 Encoder

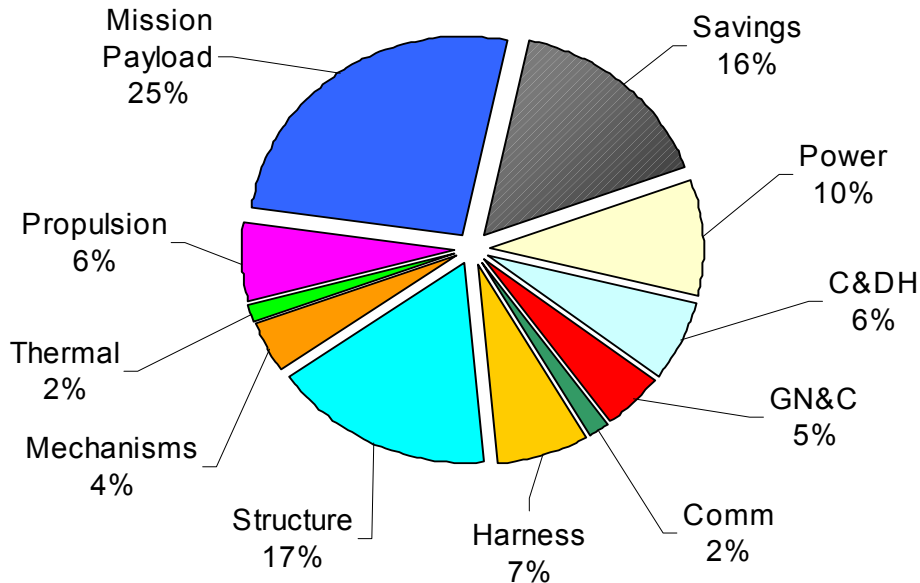
NMP EO-1 As Designed Mass



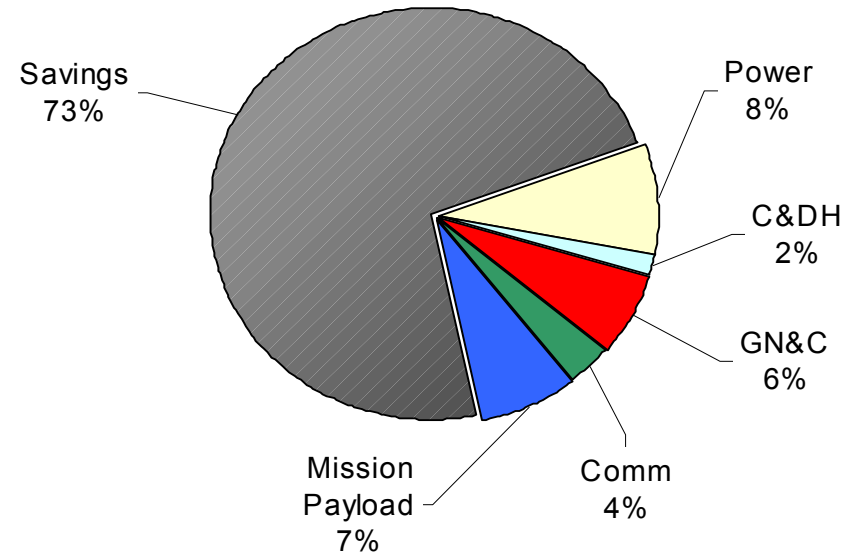
NMP EO-1 As Designed Power



NMP EO-1 Mass After ULP



NMP EO-1 Power After ULP

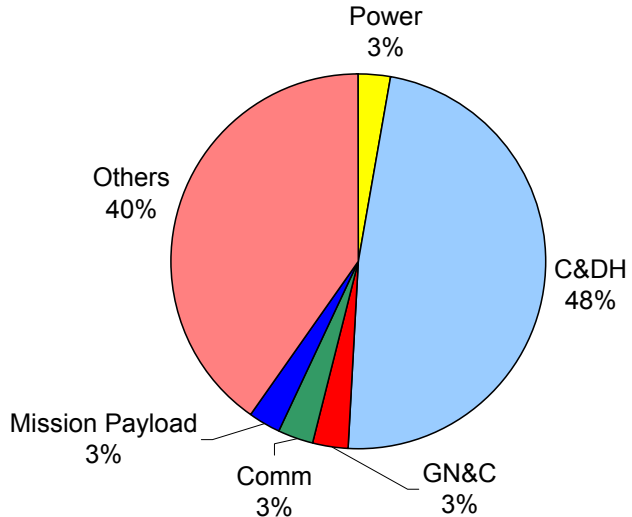




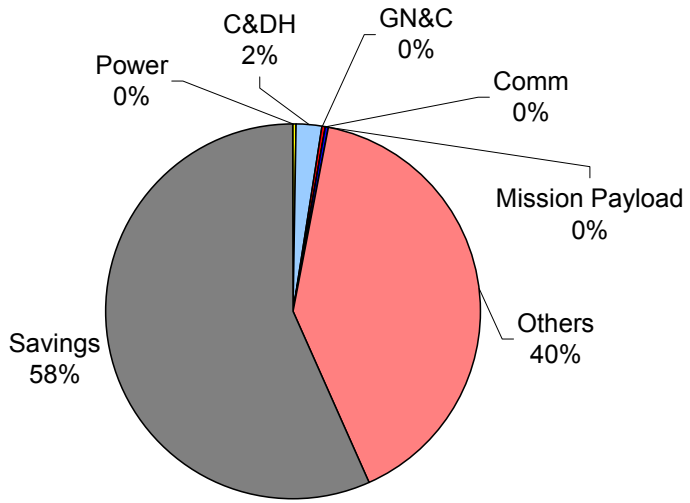
Potential Power Savings on ST5/NMP Using RT ULP

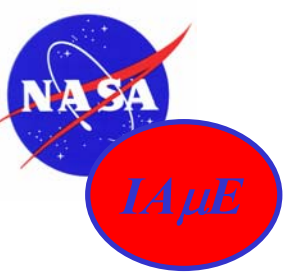


ST5 Power As Designed



ST5 Power After ULP





Conclusions

Ultra Low Power Radiation Tolerant CMOS has the potential to provide significant savings in power consumption, size, weight, and mission cost.

Up to 43X dynamic power savings possible over 3.3V parts.

ULP back-bias synergistically improves total dose hardness to 200 KRad(Si).

ULP/RT have experienced no latchup.

Low-voltage devices more susceptible to Single Event Upset.
SEU-immune latches resist latchup up to 10 MeV/mg/cm²
Improved SEU-immune cells have been designed.