

D, T and JK Constraints in Asynchronous Synthesis

David F. Cox
Research Professor
dcox@mrc.unm.edu
(505) 272-7045

NASA Institute of Advanced Microelectronics
Microelectronics Research Center
University of New Mexico
801 University Blvd. SE, Suite 206
Albuquerque, New Mexico 87106

Abstract - Low power and high speed are considered benefits in space electronics. Asynchronous circuits can provide both low power and higher speed operation in electronic circuits. Techniques are given that allow designing asynchronous circuits with the state variables being assigned to flip-flops. It is shown that any asynchronous circuit may be designed using RS flip-flops whereas D, T, and JK flip-flops may be used if certain state entry conditions are met.

1 Introduction

Asynchronous design was given a formal methodology by David Huffman in 1954 [1]. This paper will discuss extending his techniques to designs using flip-flops as the feedback elements instead of combinatorial circuits. An example design is described to provide the basis for a state diagram from which the hardware designs will be derived.

2 Example

An example design of a simple counter will be used to illustrate the techniques. The counter will count to three, have an output on the third count and then reset to begin the count. The timing diagram is given in Figure 1. Asynchronous circuits can be described, and states assigned by using timing diagrams, state diagrams or transition tables [2], [3]. This example will use a timing diagram. It should be noted that any state diagram can be used as long as it represents a legitimate sequential system. The input to this example is labeled “in” and the output is labeled “out”. The output is seen to commence with the falling of the second input pulse but could also have been simply coincident with the third input pulse.

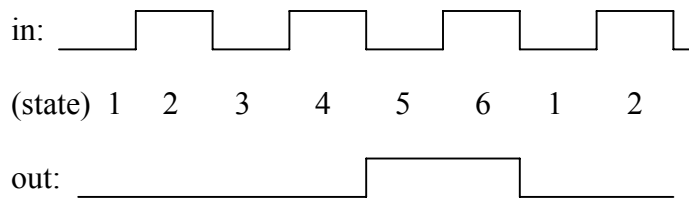


Figure 1. Timing Diagram for Counter.

The flow table and final Karnaugh map can be generated from the timing diagram as shown in Figure 2. The circled entries are stable states.

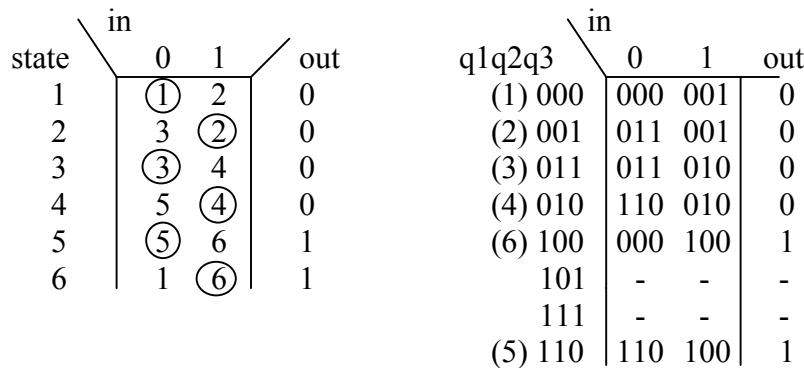


Figure 2. Flow Table and Karnaugh Map for Counter.

The states q1, q2 and q3 are then separated out into individual maps and combinatorial expressions are then generated for each of them. Each combinatorial expression will typically have feedback from the state variables.

3 RS Characteristic Equation

An implementation of the counter (or any asynchronous circuit) can be done using RS flip-flops in the following manner. The characteristic equation for the RS is generated from its characteristic map as shown in Figure 3.

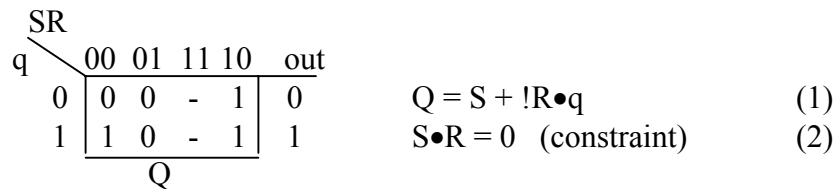


Figure 3. RS Characteristic Equation.

The counter can now be generated simply using RS flip-flops by using maps in place of the equation variables as shown in Figure 4. State variable Q1 is generated using the RS characteristic equation to determine the Set and Reset inputs [4].

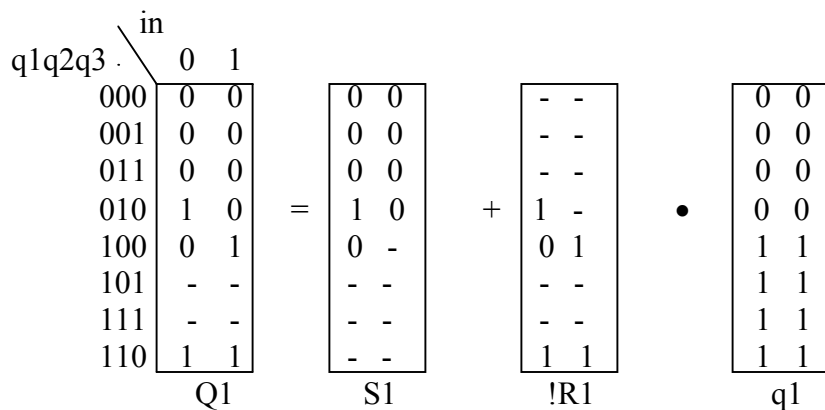


Figure 4. SR Realization for Counter Example.

S1 and R1 are filled in cell by cell to complete the equality. The map for q1 is an identity and is filled in according to what the state variable q1 is for the row. The maps are filled in with the constraint that set and reset cannot both be equal to 1 at the same time. Don't-cares can be filled in if a portion of the map completes the equation and the constraint is met. For example, the first row has “!R” anded with zeros, so its entries can be “-“ as long as the entry for S1 is a zero (which it is). The set and reset can now be found from their respective maps.

$$S1 = !in \bullet q2 \bullet !q3 \tag{3}$$

and,
$$R1 = !in \bullet !q2 \tag{4}$$

The other two state variables can be found in the same manner to complete the synthesis.

4 D Flip-Flop

Logic diagrams for the D, T and JK transition flip-flops are given in the appendix. A D flip-flop flow table can be realized from the flow table given in Figure 5. The flow table was generated by using the RS characteristic maps in reverse to generate the next-state equations [5]. The characteristic equations for the D flip-flop are given as derived from the flow table. The last term in each expression is a cover for hazards and does not need to be included in the characteristic equations because the feedback is now constrained within the D flip-flop and the design of the flip-flop itself is assumed to be hazard-free. The circled states are stable states.

The state variables can be changed to Y's so as not to confuse them with the state variables in the counter for the following synthesis. The hazard covers are ignored for reasons stated above.

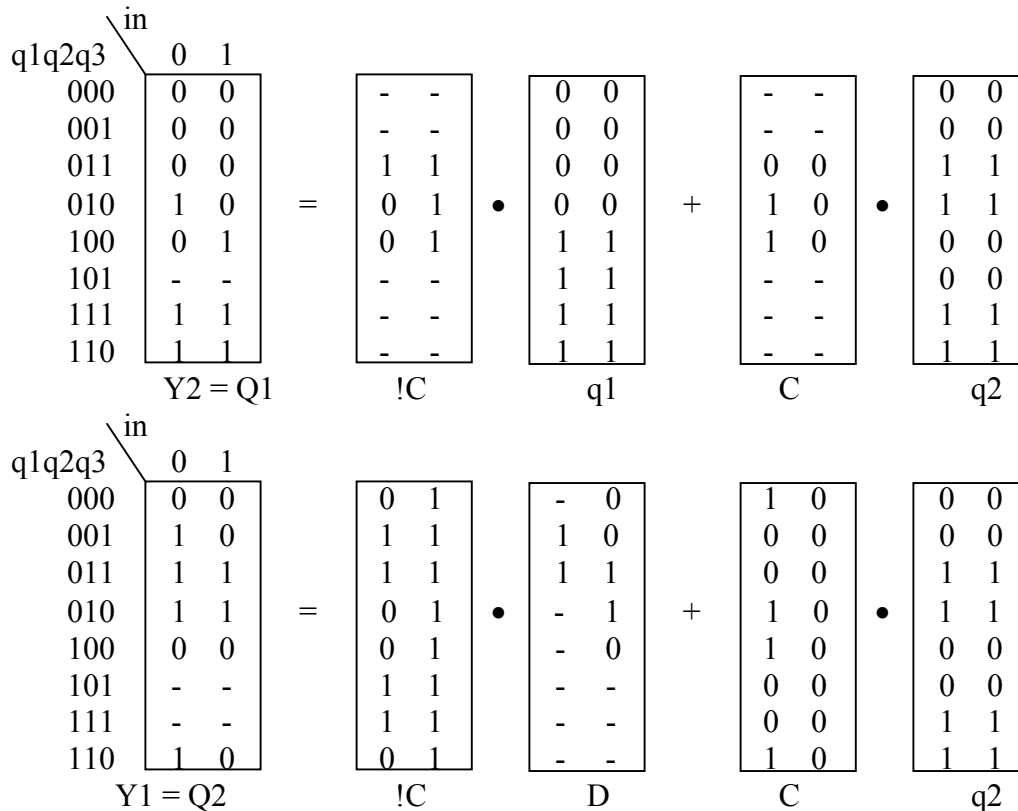
$$Y1 = !C \bullet D + C \bullet y1 \tag{5}$$

$$Y2 = !C \bullet y2 + C \bullet y1 \tag{6}$$

state (q1q2)		CD				out = q2 (=y2)	
		00	01	11	10		
1	①	4	①	①	0	$Q1 = !C \bullet D + C \bullet q1 + [D \bullet q1]$	(7)
2	②	3	1	1	1		
3	2	③	③	③	1	$Q2 = !C \bullet q2 + C \bullet q1 + [q1 \bullet q2]$	(8)
4	1	④	3	3	0		

Figure 5. D Flip-Flop Flow Table and Characteristic Equations.

It is easy to see from equations (5) and (6) or from (7) and (8) that Y2 must be equal to 0 if both y1 and y2 are 0, and that Y2 must be equal to 1 if both y1 and y2 are 1. With those constraints we can inspect the Karnaugh map for the counter (in Figure 2) and see that state variables q1 and q2 can be used for the internal variables of a D flip-flop if q1 = y2 and q2 = y1. Figure 6 shows the maps and how they are filled in. Note that the constraints are automatically met if the state variables are chosen correctly (not all maps may be synthesizable with D flip-flops). As before, q1 and q2 are identities that are filled in first. C and !C are inverses and give some flexibility on filling in the rest of the maps. Y2 is filled in first and the C-map transferred to Y1.



From which, $C = !in \bullet !q3$, (9)

and, $D = !in + q2$ (10)

Figure 6. Maps and Input Equations for D Flip-Flop in Counter Example.

Equation (10) uses state variable q_2 in the counter realization. This is typically an internal variable in a D flip-flop and may not be available. Most integrated circuit realizations of D flip-flops have the internal variables available, however, and this should not be a problem. It should be noted that q_1 is the output of the flip-flop (y_2). The third state variable, q_3 , may be realized with combinatorial logic or with an RS flip-flop. The equations for an RS implementation can be derived as before and are given in (11) and (12).

$$S_3 = in \bullet !q_1 \bullet !q_2 \quad (11)$$

$$R_3 = in \bullet q_2 \quad (12)$$

This completes the asynchronous counter design using a D flip-flop and an RS flip-flop. The rest of the discussion will describe the T and JK flip-flops but the synthesis example will not be done.

5 Non-Clocked T Flip-Flop

Figure 7 gives the flow-table, Karnaugh map and characteristic state equations for a non-clocked T flip-flop (toggle flip-flop). This would be equivalent to a D flip-flop with the T input going to the Clock and the inverse output (!Q) being fed back to the D input. The hazard cover has not been given for the reasons stated in the D flip-flop section above.

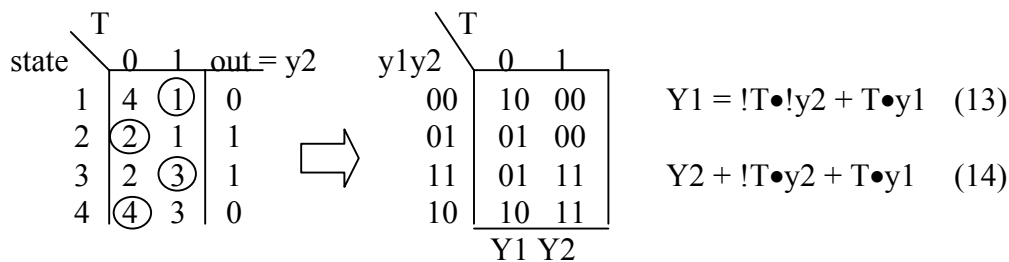


Figure 7. Non-Clocked T Flip-Flop Flow Table and Characteristic Equations.

By looking at equations (13) and (14) the constraints on the counter state variables for the example can be deduced. They are given in (15) and (16).

$$Y_1 = 1 \text{ if } y_1 = 1 \text{ and } y_2 = 0, \quad Y_1 = 0 \text{ if } y_1 = 0 \text{ and } y_2 = 1 \quad (15)$$

$$Y_2 = 1 \text{ if } y_1 = y_2 = 1, \quad Y_2 = 0 \text{ if } y_1 = y_2 = 0 \quad (16)$$

These constraints cannot be met with our present counter example with the toggle flip-flop.

6 Clocked T Flip-Flop

The flow table and next-state map for the clocked T flip-flop is shown in Figure 8. The characteristic equations are given in (17) and (18) as derived from the map.

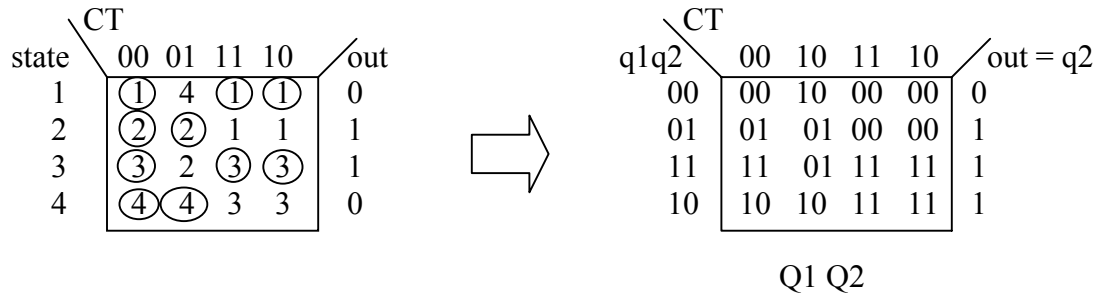


Figure 8. Clocked T Flip-Flop Flow Table and Map.

$$Q1 = C \cdot q1 + q1 \cdot !q2 + !C \cdot T! \cdot q2 + !T \cdot q1 \quad (17)$$

$$Q2 = !C \cdot q2 + C \cdot q1 \quad (18)$$

It can be seen by inspection that Q1 and Q2 have the following constraints:

$$\begin{aligned} Q1 &= 0 \text{ if } q1 = 0 \text{ and } q2 = 1 \\ &= 1 \text{ if } q1 = 1 \text{ and } q2 = 0 \end{aligned}$$

$$\begin{aligned} Q2 &= 0 \text{ if } q1 = q2 = 0 \\ &= 1 \text{ if } q1 = q2 = 1 \end{aligned}$$

These constraints make it much more difficult to fit the clocked T flip-flop into an asynchronous map without adding dummy state variables to generate extra transitions that can fill in the appropriate constraint conditions.

7 Clocked JK Flip-Flop

The JK flip-flop's flow table and next-state map are given in Figure 9. Fitting three variables (C, J and K) is going to be more difficult, in general, but the JK flip-flop has a fair amount of versatility and may be usable in more applications than the T. The characteristic equations for the JK flip-flop are given in (19) and (20), along with the map constraints.

$$\begin{aligned} Q1 &= q1!q2 + Cq1 + q1!K + !CJ!q2; \quad Q1 = 0 \text{ for } q1 = 0 \text{ and } q2 = 1, \text{ and} \quad (19) \\ & \quad Q1 = 1 \text{ for } q1 = 1 \text{ and } q2 = 0. \end{aligned}$$

$$\begin{aligned} Q2 &= !Cq2 + Cq1; \quad Q2 = 0 \text{ for } q1 = q2 = 0, \text{ and} \quad (20) \\ & \quad Q2 = 1 \text{ for } q1 = q2 = 1. \end{aligned}$$

state	JK C=0				JK C=1				out
	00	01	11	00	00	01	11	10	
1	①	①	4	4	①	①	①	①	0
2	②	②	②	②	1	1	1	1	1
3	③	2	2	③	③	③	③	③	1
4	④	1	④	④	3	3	3	3	0

q1q2	JK C=0				JK C=1				out=q2
	00	01	11	10	00	01	11	10	
00	00	00	10	10	00	00	00	00	0
01	01	01	01	01	00	00	00	00	1
11	11	01	01	11	11	11	11	11	1
10	10	00	10	10	11	11	11	11	0

Q1 Q2

Figure 9. JK Flip-Flop Flow Table and Map.

The JK flip-flop constraints for Q2 are the same as the D flip-flop Q2 constraints but the JK has an added constraint on Q1 which the D does not have.

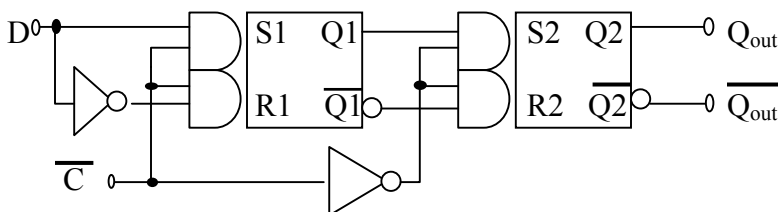
8 Conclusions

A method has been presented to allow realizations of asynchronous systems using RS and transition flip-flops. The RS is seen to be capable of realizing any asynchronous flow table without modification of the table. A simple constraint equation is seen to be easy to achieve by filling out the set and reset maps accordingly. The transition flip-flops require two characteristic equations for their description and the constraint equations place actual constraint values on the state variables in the asynchronous map that are to be synthesized with the flip-flop. These constraints can sometimes only be achieved by adding extra state variables and using transition states to conform to the constraints. It should be noted that glitches on the D, T, J or K inputs may cause improper master latching when the clock is low. This can be corrected by altering one or two of the next-state sequences in the flow table. The net result would be a slightly more complex, but more robust, flip-flop.

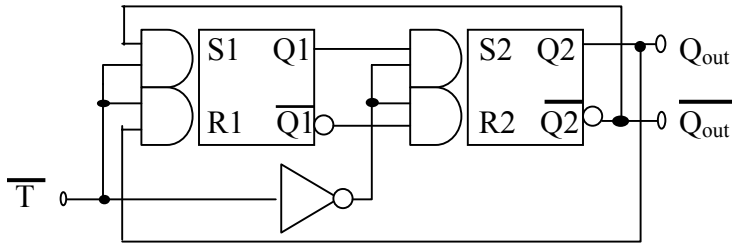
These techniques may be used in designing lower-power and higher-speed digital systems for use in space systems where radiation is also a problem [6]. Known radiation-tolerant design techniques [7] can be used in the design of the flip-flops to insure robust operation in a space environment.

APPENDIX

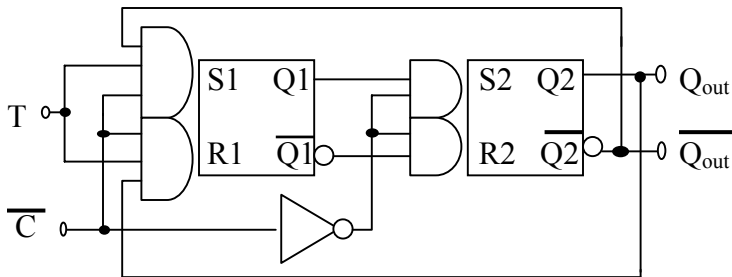
D Flip Flop Realization



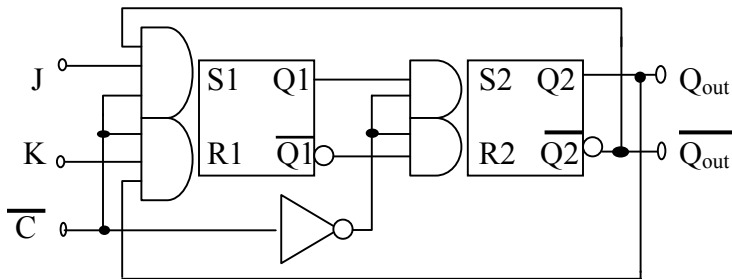
Non-Clocked T Flip-Flop Realization



Clocked T Flip-Flop Realization



JK Flip-Flop Realization



References

- [1] David A. Huffman, "The Synthesis of Sequential Switching Circuits", Journal of the Franklin Institute 257 (3), pp. 161-190, 257 (4), pp. 275-303, 1954.
- [2] M. Morris Mano, "Digital Design", Second Edition, Prentice-Hall, 1991.
- [3] Stephen H. Unger, "Asynchronous Sequential Switching Circuits", John Wiley & Sons, Inc., 1969.
- [4] D.F. Cox, "Asynchronous Logic Design with Transition Flip-Flops", IEEE Midwest Symposium on Circuits and Systems, August, 1999, Los Cruces, New Mexico.
- [5] D. F. Cox, "Asynchronous Logic Design with Subcells", 6th IEEE International Conference on Electronics, Circuits and Systems, September, 1999, Pafos, Cyprus.
- [6] T. P. Ma and Paul V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", John Wiley & Sons, 1989.
- [7] J. Canaris and S. Whitaker, "Circuit Techniques for the Radiation Environment of Space", IEEE 1995 Custom Integrated Circuits Conference, pp. 5.4.1 – 5.4.4, 1995.