

Cryogenic Operation of Ultra Low Power CMOS¹

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Abstract – This paper explores the use of an ultra low power (ULP) CMOS technology at cryogenic temperatures. ULP CMOS has demonstrated order-of-magnitude savings in power for complex circuits and may be well suited for applications where electronic circuits must operate at cryogenic temperatures. Simple ULP test structures were tested at temperatures as low as 15 K.

1 Introduction

Ultra low power (ULP) CMOS has been demonstrated at supply voltages of 0.5 V for complex circuits such as Reed-Solomon encoders and at voltages as low as 0.2 V for simple circuits. This technology offers potential power savings of up to a factor of 100 over conventional CMOS operating at 5 V and has shown a power savings factor of over 35 for the same device operating at 3.3 V. ULP operation is a distinct advantage for cryogenic applications because the need to eliminate waste heat is also greatly reduced. However, CMOS circuits behave much differently at very low temperatures and can have lower reliability than circuits operating at conventional temperatures. In order to gain a preliminary understanding of the suitability of ULP CMOS to cryogenic applications we tested a simple ULP circuit at 15 K.

2 Ultra Low Power CMOS

The total power consumed in CMOS digital systems has two major components

$$P_{TOTAL} = P_{DC} + P_{AC}$$

where P_{DC} is the power consumed under quiescent d.c. conditions and P_{AC} is the power consumed by switching the inherent load capacitances in the system. There is a third component due to short circuit current through switching transistors, but this can usually be neglected in properly designed circuits. P_{DC} is simply the product of the power supply voltage and the transistor leakage current. P_{AC} is equal to the supply voltage multiplied by the average current needed to charge or discharge the load capacitance. In this context, the load capacitor is the sum of all internal wiring and gate capacitance within the integrated circuit. The average current needed to charge a capacitor is equal to the product of the capacitance and the magnitude of the voltage change, which is typically equal

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to the supply voltage, multiplied by the frequency that the capacitor is charged or discharged. With these substitutions the power equation becomes

$$\begin{aligned} P_{TOTAL} &= (V_{SUPPLY} \times I_{LEAK}) + (V_{SUPPLY} \times I_{CHARGE}) \\ &= (V_{SUPPLY} \times I_{LEAK}) + (V_{SUPPLY}^2 \times C_{LOAD} \times F_{CLOCK}) \end{aligned}$$

When F_{CLOCK} is small the d.c. component of power consumption is dominant. In this case it is desirable to minimize I_{LEAK} by manufacturing CMOS transistors with a high threshold voltage. Unfortunately, relatively high supply voltages are then needed to maintain an acceptable level of performance. When F_{CLOCK} is large the a.c. component of power consumption becomes dominant, and the power consumption of CMOS circuits rivals that of “power hungry” bipolar technologies. Efforts to reduce C_{LOAD} or F_{CLOCK} can achieve significant reductions in power, but reducing V_{SUPPLY} is a much more powerful approach since this term is squared in the a.c. power component.

However, in order to maintain a high level of performance at reduced supply voltage, V_{DD} , the transistor threshold voltage, V_T , must be correspondingly reduced. Digital logic typically uses a $V_{DD} : V_T$ ratio of 3 to 5 for high performance while maintaining adequate noise margins. For a V_{DD} of 0.5 V this would suggest that a V_T of 0.1 V to 0.17 V is needed. Unfortunately, the variation in V_T due to manufacturing, temperature, and other environmental effects is relatively large at these levels and would make it very difficult to design conventional circuits that can be manufactured with high yield and used in a broad range of conditions.

One solution to this problem is to abandon the notion of the transistor threshold as a fixed parameter. By actively controlling the transistor thresholds we can compensate for the variability described above and allow device operation at very low supply voltage. This is made possible by first building transistors with intrinsic, or native, thresholds that are very near zero. The connections to the transistor bodies, either through the substrate or implanted wells, are then maintained separate from the V_{DD} and V_{SS} supply lines. By bringing these body connections to two external pins a *back bias* voltage can be applied. The bias voltage has a polarity that will create a reverse bias at the source/body junction, and the operational threshold voltage can be increased by increasing the magnitude of the bias. Thus, the threshold voltage can be controlled in real time during circuit operation. Typical I/V curves for such a transistor at room temperature are shown in Figure 1.

3 Considerations for Cryogenic Operation

As CMOS operating temperatures are lowered to around 100 K these circuits will continue to exhibit the temperature effects that are seen near room temperature. Carrier mobility increases as the temperature is lowered and scattering within the silicon lattice is reduced. Intrinsic transistor thresholds also increase with reduced temperature [1]. The variations in threshold voltage and mobility are opposing forces, with lowered mobility tending to improve transistor drive while increased threshold voltages will degrade transistor drive. Conventional CMOS transistors have a peak linear drain current at about 100 K [2].

At temperatures below 100 K the behavior of CMOS devices becomes more difficult to predict. The effect known as *impurity freeze out* begins to appear and limit performance [2–4]. Impurity freeze out occurs when the dopant atoms implanted in the silicon do not ionize readily, which

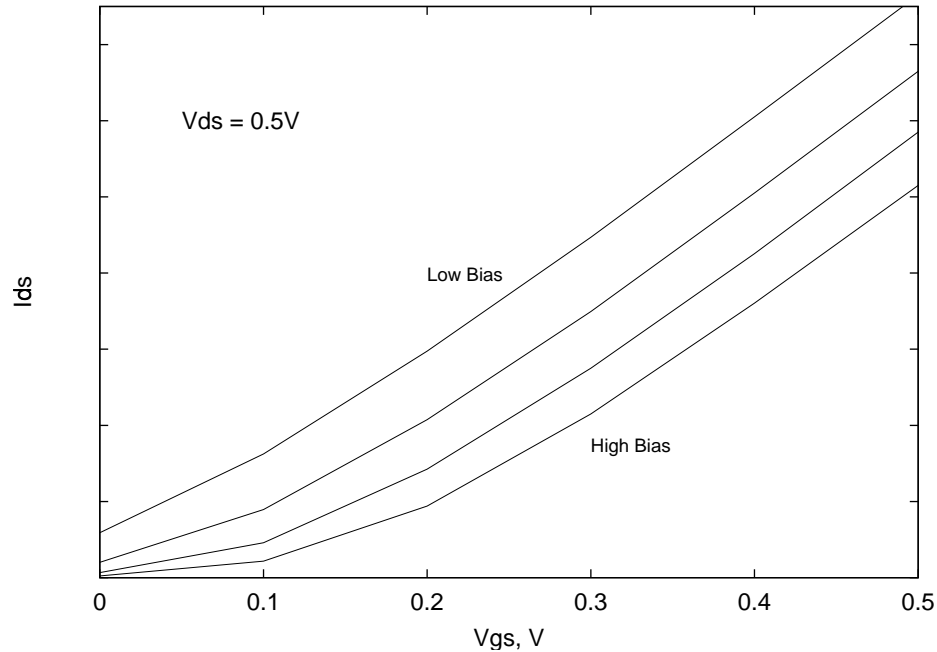


Figure 1: ULP NMOS Transistor I_{DS} vs. V_{GS}

dramatically decreases the conductivity of lightly doped regions. The degradation in transistor performance can be severe if lightly doped drains (LDD) are used. These structures are typically added to reduce hot carrier effects, which can greatly degrade the reliability of modern submicron devices.

Hot carrier effects occur during the switching of a transistor, when a channel is forming with a high voltage at the drain. Very high fields exist between the drain and the end of the channel, causing carriers to be accelerated to very high energies. These carriers can be injected into the gate oxide where they cause permanent shifts in the transistor threshold. While most reliability phenomena are accelerated by increasing temperature and of less concern at cryogenic temperatures, hot carrier effects are worsened at low temperature because the carriers have greater mobility and will travel farther before colliding with the silicon lattice [5]. Thus, conventional CMOS devices must sacrifice either reliability or performance at cryogenic temperatures. Fortunately, ULP transistors do not subject the drain to high voltages and therefore do not need LDD structures.

Impurity freeze out can also occur when the transistor gate polysilicon is doped with the opposite type of the desired transistor, as is common in many CMOS processes [6]. For example, if a PMOS transistor has an n+ gate polysilicon then conduction will actually occur somewhat below the surface of the silicon, in a *buried channel* that is susceptible to carrier freeze out. The ULP process requires that polysilicon gates be doped like the underlying transistor in order to achieve near zero thresholds, so this desirable trait for cryogenic applications is inherent in ULP technology.

Finally, a transistor's subthreshold slope becomes steeper at low temperature and hence its leakage current in the off state decreases significantly [1, 2, 6]. This effect should allow circuit operation with lower threshold voltages without increasing the d.c. component of the total power [7].

4 Preliminary Test Results

Previous cryogenic ULP testing explored the behavior of these circuits at the temperature of liquid nitrogen, 77 K [8]. Many space applications require operation at substantially lower temperatures, so the goal of this work was to obtain data on ULP test circuits at 15 K. Conducting tests at this temperature is considerably more difficult than testing with liquid nitrogen. For our preliminary testing we used a very simple test structure: a ring oscillator formed from 49 inverters, as shown in Figure 2. The inverters in the oscillator have very small transistors, which does not represent a normal design style for an application circuit. On the contrary, the oscillator is designed to be very sensitive to small changes in circuit parameters. One of the ULP test chips that has been manufactured contains two of these oscillators on each die.

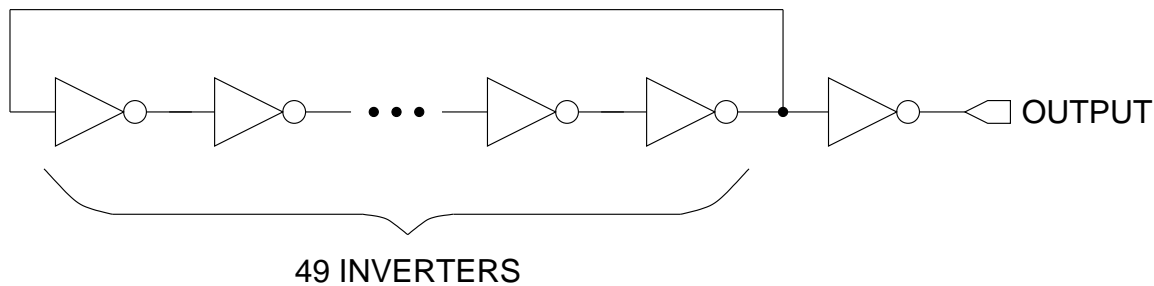


Figure 2: Ring Oscillator Test Circuit

The device under test was mounted to the second stage of a two stage Gifford-McMahon cryocooler and cooled to approximately 15 K under a vacuum level of less than 10^{-6} torr. Temperature and vacuum measurements were acquired using silicon diodes and a Bayard-Alpert ionization gauge, respectively. An automated Labview based data acquisition system was utilized to capture cryogenic temperature readings.

The data from testing both of the oscillators on one test chip is shown in Figures 3 through 5. Figure 3 shows how the average oscillation frequency of the two oscillators changed as the device temperature was gradually lowered. There may be significant noise in this data, but there is clearly an indication that the performance of the oscillators reaches a peak in the vicinity of 150 K. However, we do not see the large increases in performance that are often observed in conventional CMOS. The ULP circuits tested here were designed to have near-zero transistor threshold voltages at room temperature, which likely results in a threshold voltage that is much larger than desired when these circuits are operated at cryogenic temperatures. Since the ULP circuits are operated at only 0.5 V they tend to be more sensitive to threshold variations, and for optimum performance at very low temperature the process should be tuned to provide near-zero intrinsic thresholds at the desired operating temperature. Nevertheless, the existing ULP process provides a level of performance that may be adequate for many applications.

One concern that arose was that impurity freeze out might make it difficult or impossible to control the transistor thresholds with a back bias. The substrate and wells are lightly doped and may have a very low conductivity. The data in Figure 4 shows that these fears were unfounded. The behavior of the oscillators at 15 K as a function of bias is very similar to their behavior at room temperature. The measured power consumption of the oscillators is shown in Figure 5. The data points at zero bias are consistent with the expectation that leakage current, which is very significant

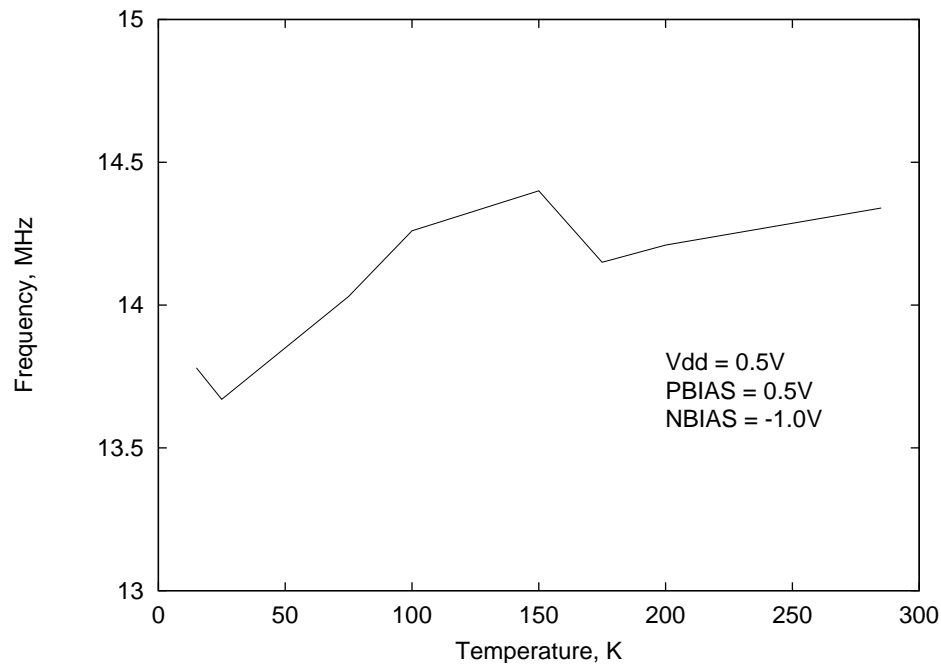


Figure 3: Ring Oscillator Frequency vs. Temperature

at low bias voltage, has been reduced because of the increased subthreshold slope. Unfortunately, ring oscillators do not allow the static leakage current to be measured directly. The measurements at higher biases suggest that the ULP circuits consume more power at cryogenic temperatures, which is counterintuitive. Note however that these differences are tens of nanowatts, and more complex circuits may be needed to make meaningful and reliable power comparisons.

5 Conclusion

Ultra low power CMOS appears to function well at cryogenic temperatures as low as 15 K. There is little performance degradation with respect to room temperature operation and the back bias voltage is an effective means for controlling transistor thresholds. Additional testing is indicated, using a variety of test circuits as well as complex functional designs. Individual transistors should be characterized at these temperatures to measure the variation in threshold voltage, mobility, and channel resistance.

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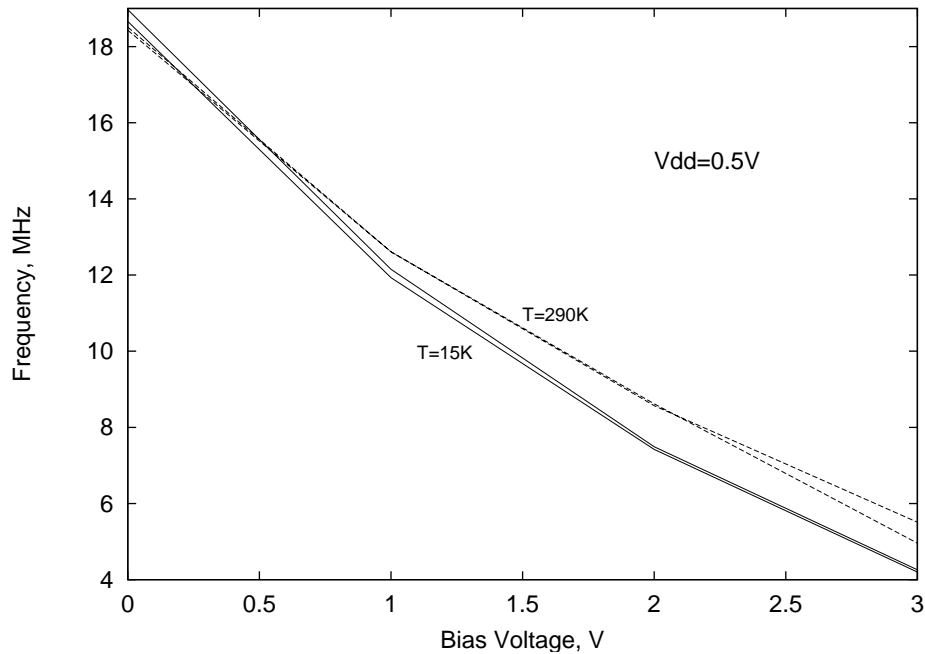


Figure 4: Ring Oscillator Frequency vs. Bias Voltage

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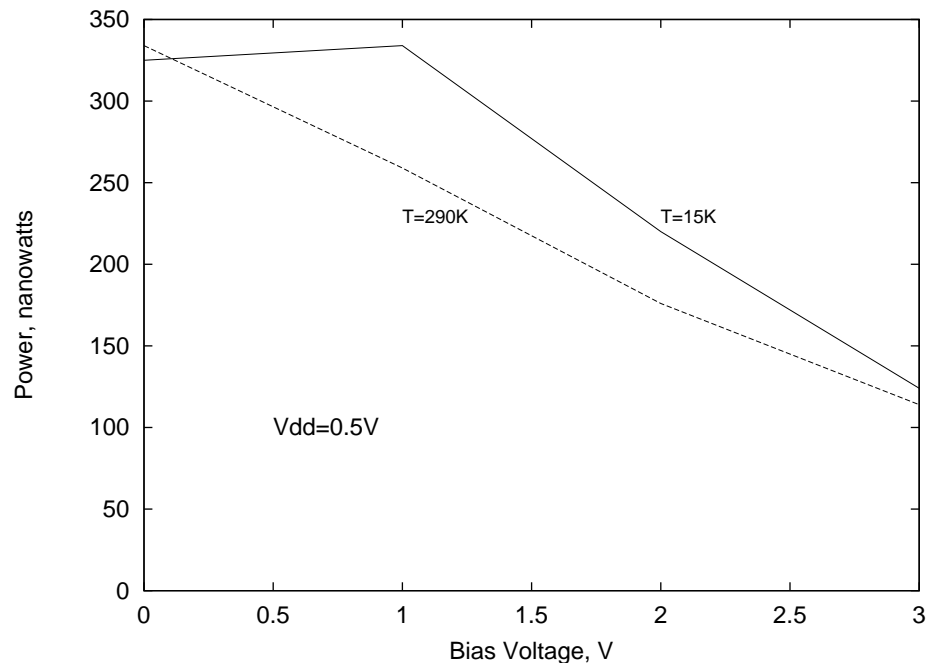


Figure 5: Ring Oscillator Power vs. Bias Voltage

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