Logic Design Considerations for 0.5-Volt CMOS

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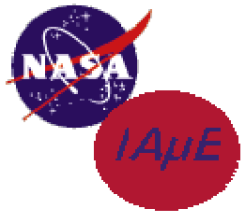

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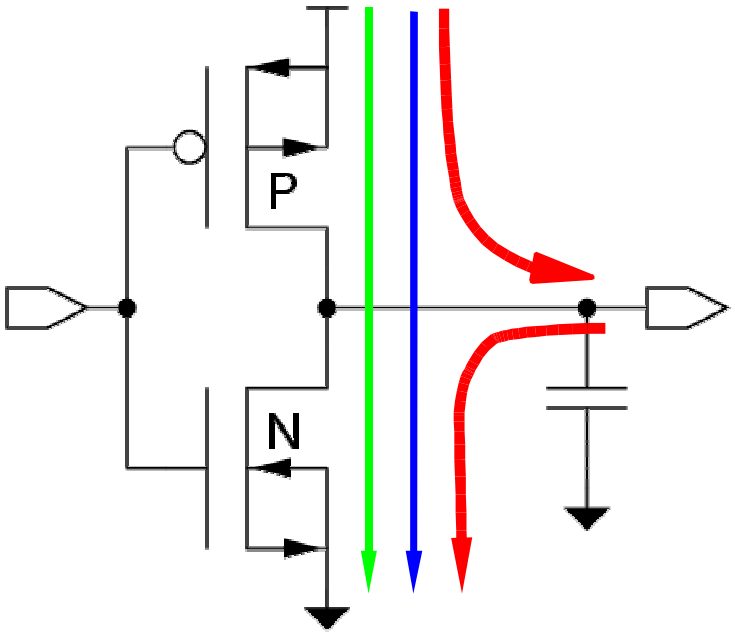
Logic Design Considerations for 0.5-V CMOS

- Low voltage CMOS technology
- Unique design considerations at 0.5-Volt
- Design Examples
  - Latches and Flip Flops
  - Multiplexers
  - Memories

Power Dissipation in CMOS

- Short-circuit or shoot-through current
  - Both transistors conduct during switching event
  - Usually negligible in well designed circuits
- Static leakage current
  - Subthreshold leakage in transistors
  - Negligible in traditional CMOS
- Switching current
  - Power proportional to $V^2C_{LOAD}F_{CLOCK}$
  - Predominates in traditional CMOS



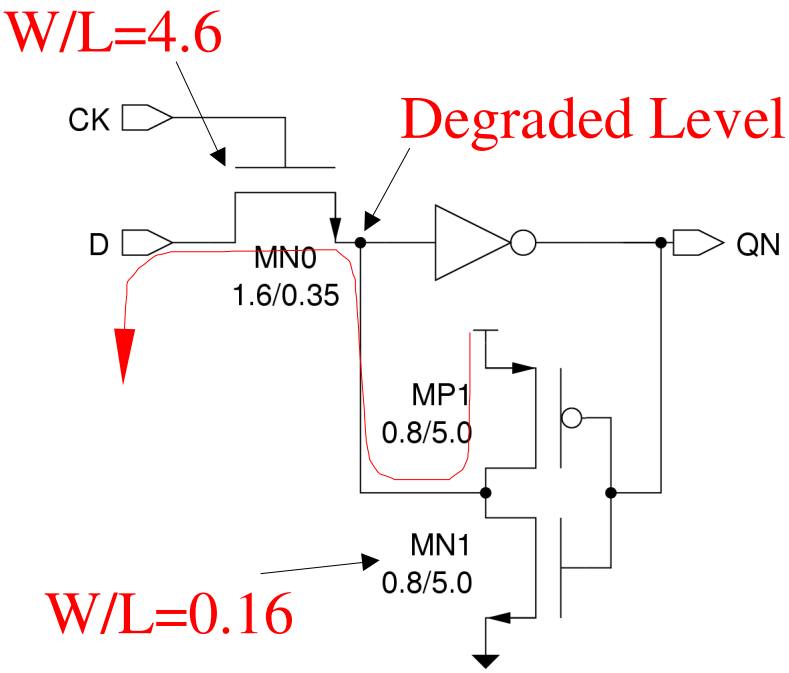
Reducing Power by Reducing Voltage

- At high clock frequencies the dynamic power in conventional CMOS is orders of magnitude larger than the leakage power
- Reducing the supply voltage can provide dramatic reduction in power dissipation, $\propto V^2$
- Transistor threshold voltage must also be reduced to maintain switching speed, $V_{DD} \approx 3 \times V_{TH}$
- Subthreshold leakage increases at low V_{TH}
- *Optimum point is where dynamic power equals static leakage power*

Consequences of Reducing Supply Voltage

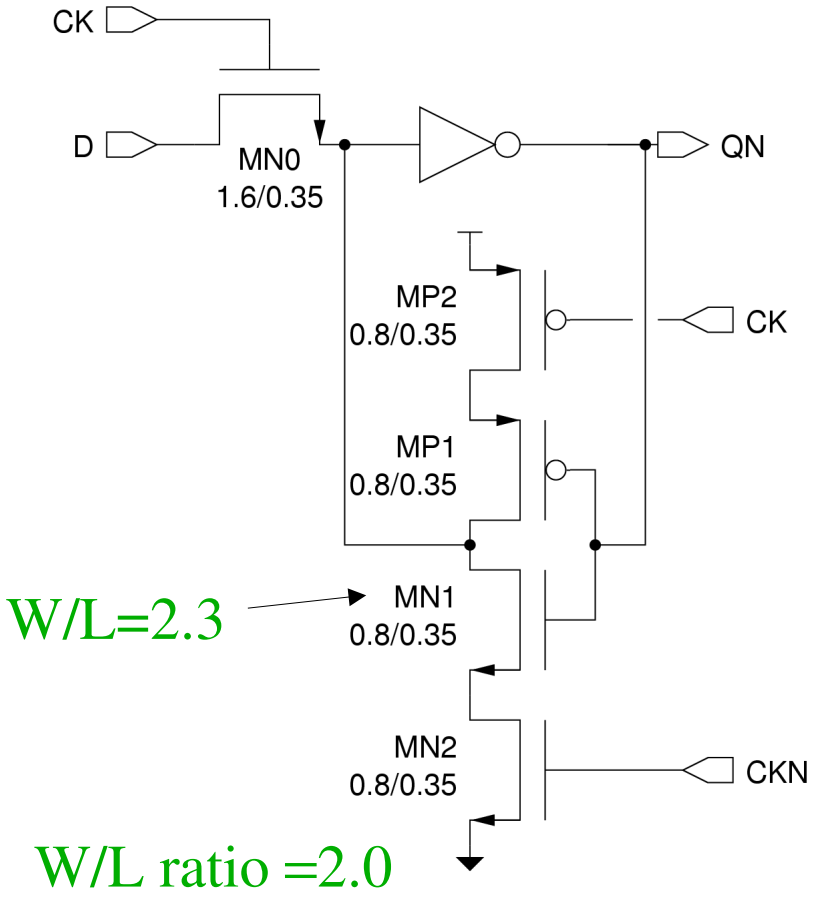
- Transistor leakage current is not negligible
  - Floating nodes don't float for long
  - Circuits requiring specific transistor ratios may fail
  - Multiple parallel transistors can be a problem
  - Logic levels can be degraded
- Transistor threshold variation is not negligible
  - Active control needed to adjust thresholds to compensate for temperature, manufacturing, etc.
  - Circuits must be robust to threshold variations across a single die

Leakage Problems in Latches



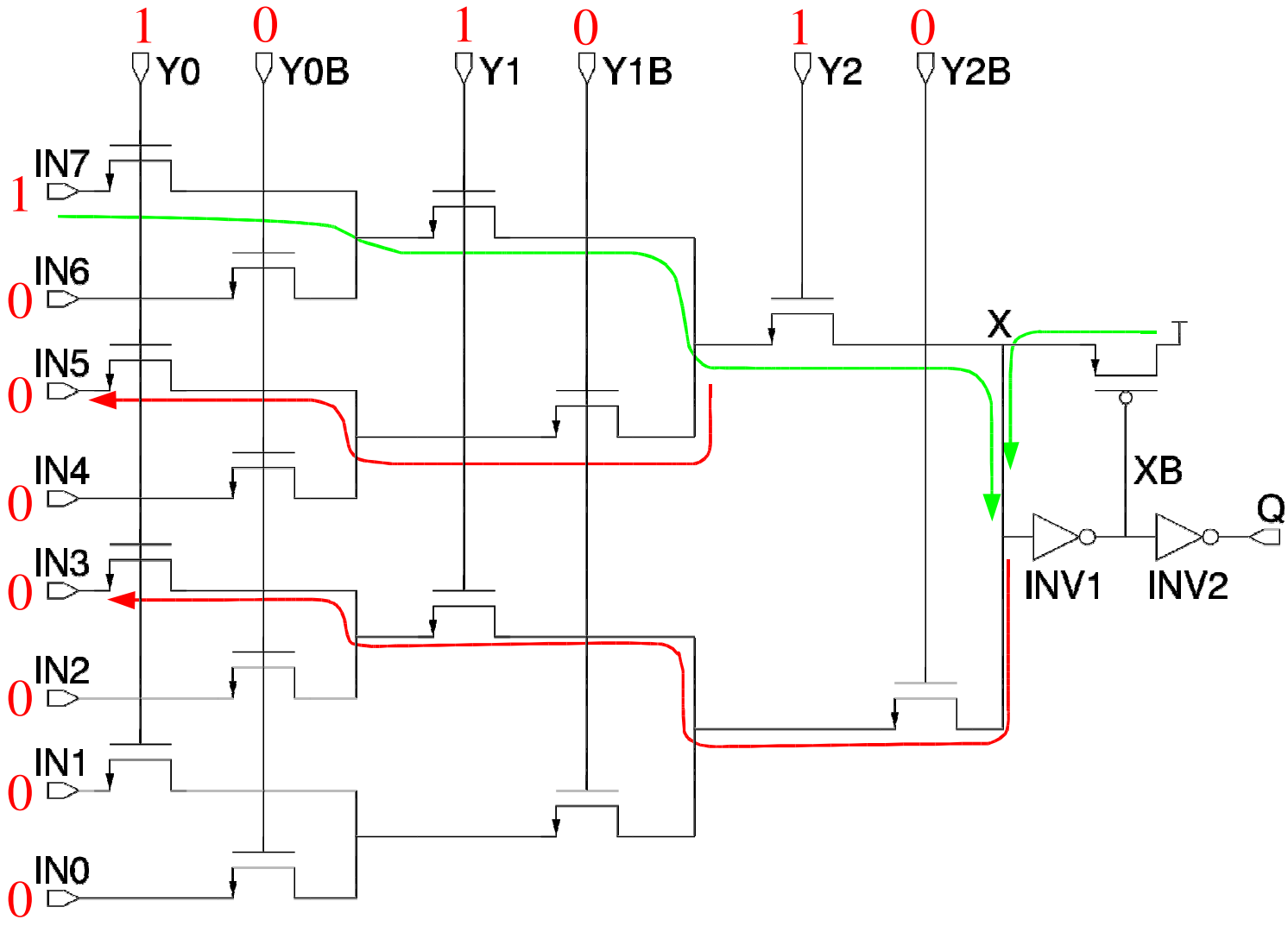
W/L ratio ≈29

This circuit fails when I_{ON}/I_{OFF} is low

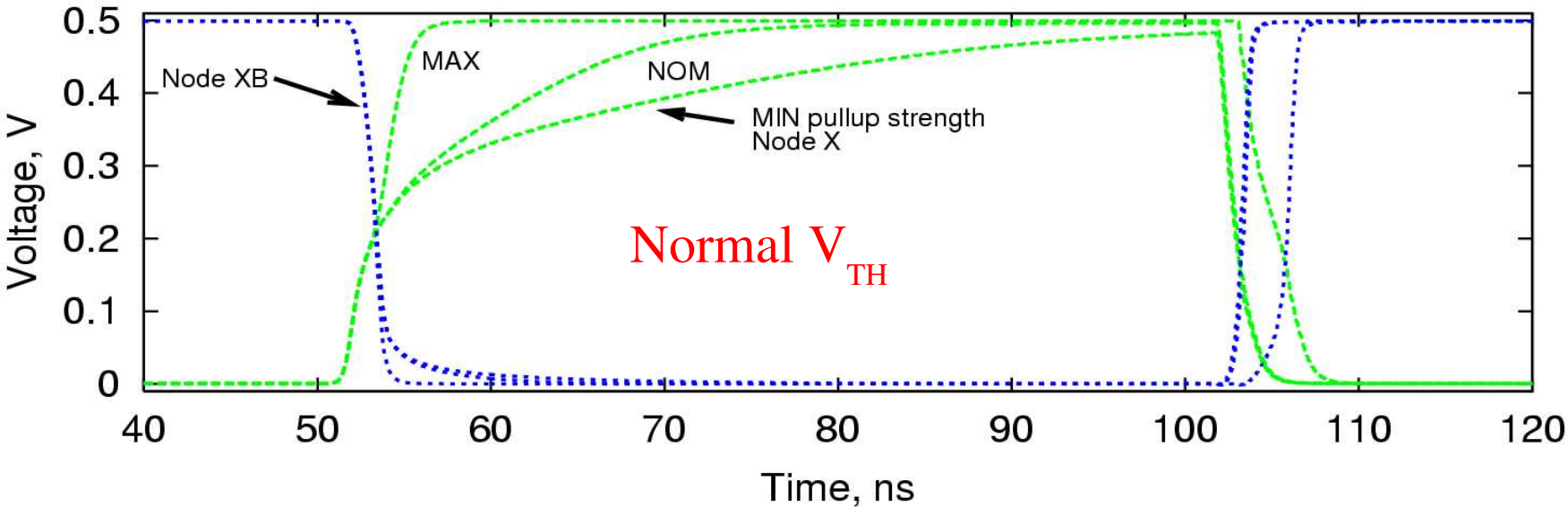


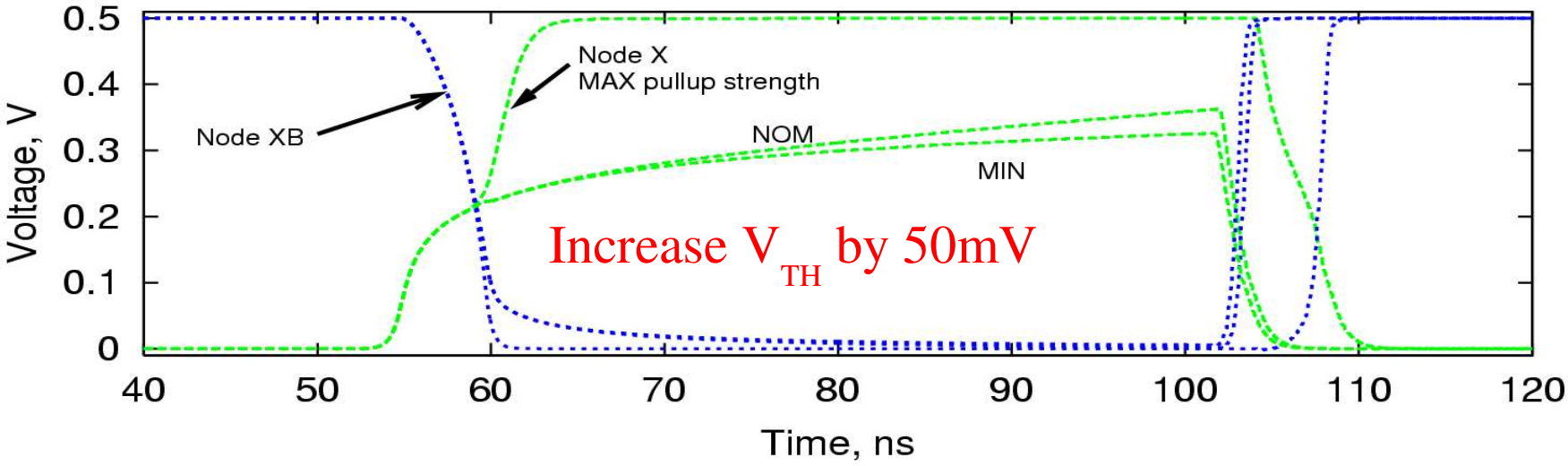
Improved Circuit Design

Transistor Ratio Problems in Multiplexers

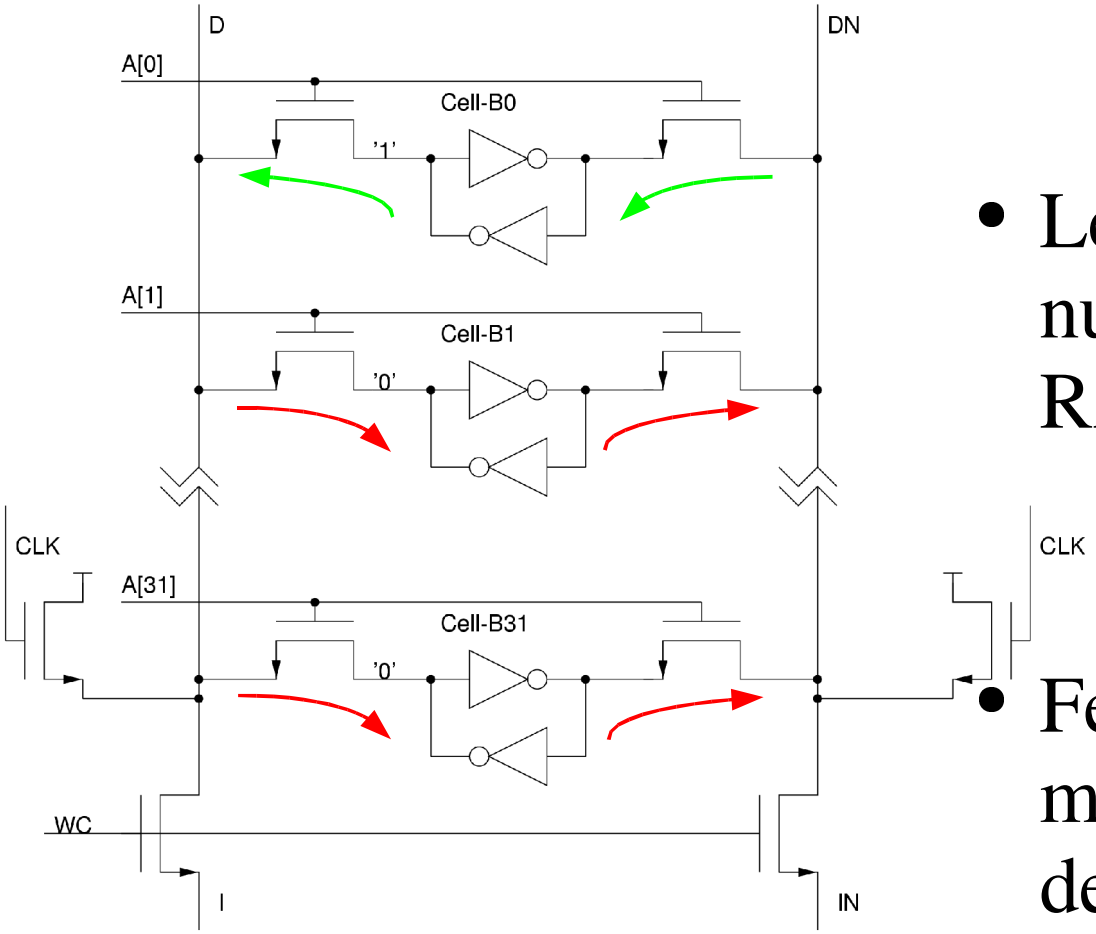


Transistor Ratio Problems in Multiplexers





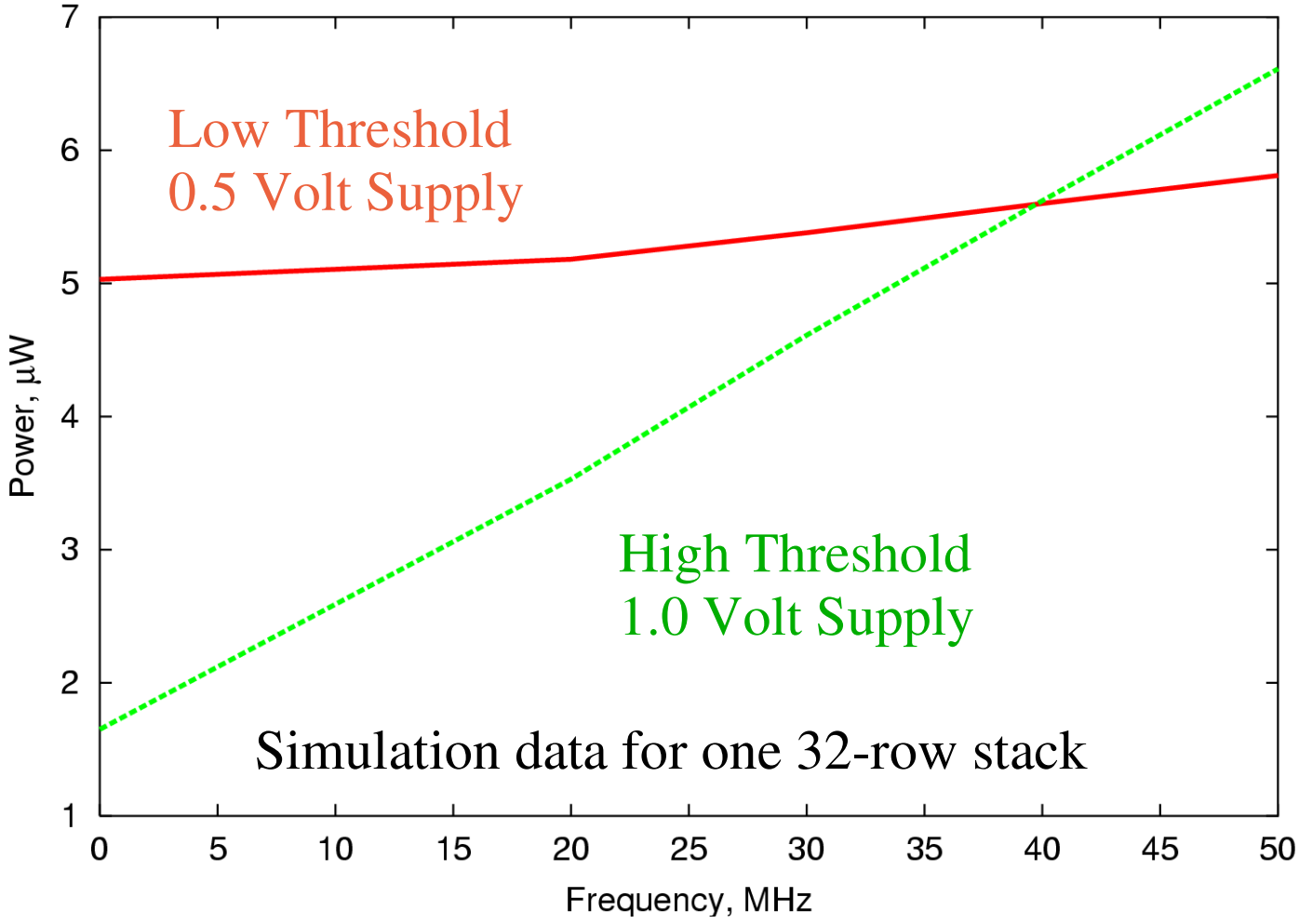
Leakage Tradeoff in RAMs



- Leakage current limits number of rows per RAM block
- Fewer rows means more blocks, more decoding logic

Tradeoff between power lost due to leakage and power consumed by additional decoders must be made

Threshold/Supply Voltage Tradeoff



Use highest threshold and lowest supply voltage that meets performance requirements

Conclusions

- Dramatic power reduction can be achieved by operating at low supply voltage
- With low thresholds transistors do not behave as ideal switches
  - Subthreshold Leakage
  - Threshold Variation
- Dynamically adjusted thresholds provide an additional degree of freedom for the designer