Mitigating Single Event Upsets From Combinational Logic [1]

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Abstract – **Novel techniques for mitigating single-event upsets originating in combinational logic have been implemented in a low-power, 0.5μm standard cell library. This method relies on a unique latch circuit, but is compatible with common CMOS processes. Combinational logic cells are also optimized to minimize pulse spreading. The results of heavy ion testing show that SEU originating in combinational logic can be a significant threat, and that these techniques are effective in reducing the occurrence of those upsets.**

1 Introduction

Single-event upsets (SEU) that are caused by cosmic particle strikes to combinational logic have been observed and studied by several researchers [1–4]. These upsets can occur when a particle strikes a combinational logic node and creates a temporary voltage disturbance at that node. If the voltage disturbance propagates to a latch and occurs near the clock edge then the disturbed state may be loaded into the latch, causing the stored data to be incorrect just as if the latch itself were struck by a cosmic ray and changed state. In the example shown in Figure 1, the correct state of the D input is a 0, but a momentary disturbance to the 1 level is latched and causes an SEU.

There is a consensus that the incidence of such upsets increases linearly with clock frequency, so that low frequency SEU testing is likely to underestimate their significance. Laser simulations suggest that at high clock frequencies the contribution of upsets from combinational logic may even exceed that of memory elements such as latches and flip flops [5]. This problem is likely to be more significant in sub-micron process technologies, because parasitic bipolar effects cause charge collection to continue for a longer period of time, leading to

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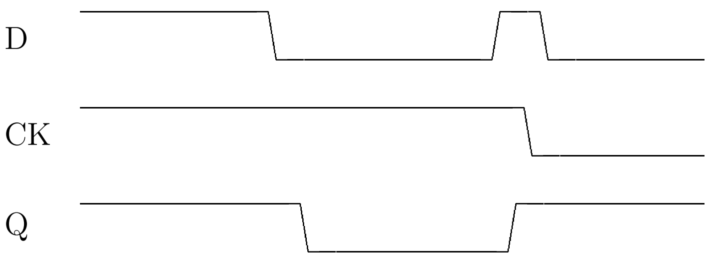

Figure 1: Transient Disturbance Causing SEU in Conventional Latch

more significant voltage disturbances [6]. Also, as transistors are scaled to deep sub-micron levels at lower operating voltages the amount of charge collected from a particle hit does not decrease as rapidly as the amount of charge needed to cause upset [7].

Previous efforts to avoid upsets from combinational logic have relied largely on “brute force” approaches, where very large transistors are used to absorb all deposited charge or where critical signal nodes have a high capacitance to minimize any voltage disturbance. The problem can also be attacked at the architectural level by providing three fully redundant logic blocks with voting circuits.

This paper describes a new technique for mitigating single-event upsets from combinational logic, which is compatible with typical commercial integrated circuit design and manufacturing methods. The foundation of this approach is a unique SEU-tolerant latch, which can ignore transient errors on its data input. In addition, the logic gates used to form combinational blocks have been optimized to reduce the severity of single event transients. These techniques have been embodied in a commercial standard cell family, and are being characterized for 0.5μm and 0.35μm CMOS processes.

2 SEU-Tolerant Circuit Design

The techniques described here for mitigating SEU caused by particle strikes to combinational logic rely on the unique properties of an SEU-tolerant latch. The transistor schematic for the basic latch cell is shown in Figure 2. The latch has two complementary clock inputs, CK and CKN. There are also two data inputs, DP and DN, which have the same polarity. These two inputs drive the upper, PMOS-only, section of the latch and the lower, NMOS-only, section respectively. The simplified schematic given here illustrates a single latch circuit with a Q output, but more complex structures such as edge-triggered flip flops are easily created from this latch. The inherent SEU-resistance of this circuit has been described, and it has demonstrated high immunity to SEU caused by cosmic particle strikes [8–10]. The design is robust and has been implemented in several commercial CMOS processes [11]. A variety of special purpose processors developed using this design have been successfully deployed in space, on missions such as the Hubble Space Telescope [12].

The critical characteristic of the latch for this discussion is that once it has stored a correct state, then an incorrect transition on either data input alone will not cause the latch

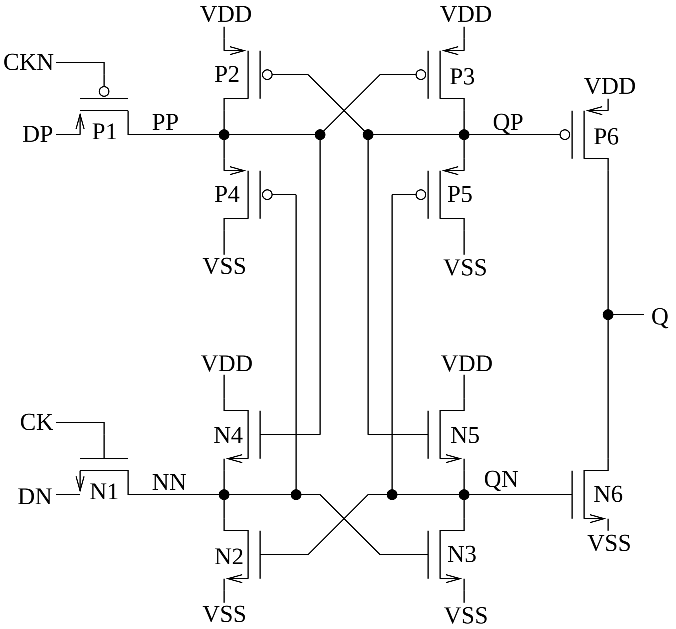

Figure 2: SEU Tolerant Latch

to change state. For example, suppose that a logic 0 is to be stored in the latch. A low level is asserted on the DP and DN inputs while the clock inputs are asserted (CKN to a 0 and CK to a 1). Transistors N2 and N4 are relatively weak in comparison to the input pass transistor N1 (as are P2 and P4 in comparison to P1) so nodes PP and NN are also brought to a 0 level. The low level at PP enables transistor P3, which brings node QP high and disables the PMOS output driver, P6. N4 is also disabled, allowing node NN to remain low. The low level at NN disables transistor N3. Since node QP is high transistor N5 will be enabled, bringing node QN high and enabling the NMOS output driver, N6, so that the Q output is asserted to a 0. The latch quickly settles to a stable state with P4 and N2 enabled while P2 and N4 are disabled, reinforcing and maintaining the 0 state at nodes PP and NN. Similarly, P3 and N5 are enabled while P5 and N3 are disabled, thus maintaining the 1 state at nodes QP and QN. If the clock inputs are now deasserted the latch will maintain the correct state.

Suppose that the latch has assumed the correct state and the clock inputs remain asserted. If the DN input is driven to the incorrect 1 state then node NN will also rise, enabling transistor N3. Transistors N5 and P5 are relatively weak in comparison to N3 and P3, respectively, so transistor N3 will bring node QN low, disabling transistor N6. Transistor P5 will also be enabled but it is unable to over drive transistor P3 and bring node QP low, so output transistor P6 remains disabled. In this situation both of the output transistors are disabled and the correct output state is maintained by the parasitic capacitances present on the Q output. If the incorrect state on the DN input is brief, as would be the case if it were caused by a cosmic particle strike, then the latch will return to the correct internal state without any change in the logic level of the Q output. Careful selection of the transistor size ratios can also prevent the latch from changing to an incorrect state if the clock inputs are deasserted while one of the inputs is in a brief incorrect state.

An obvious method for exploiting this behavior in the latch is to provide two redundant logic blocks to create the DP and DN inputs. While this is less expensive than implementing full triple redundancy, it is still a significant burden and is not compatible with commercial high-level synthesis methods. The work described here replaces the functional separation of redundant logic blocks with a *temporal separation* technique. Temporal separation separates the two latch inputs in time, so that a transient voltage disturbance does not appear at both inputs simultaneously. This is accomplished by adding a delay element between the inputs, so that the DP input becomes the normal D input to the latch while the DN input is fed a delayed version of the DP signal, as shown in Figure 3. To the first order, temporal separation enables the latch to ignore transient pulses whose duration, TW, is less than the propagation delay through the delay element, TD.

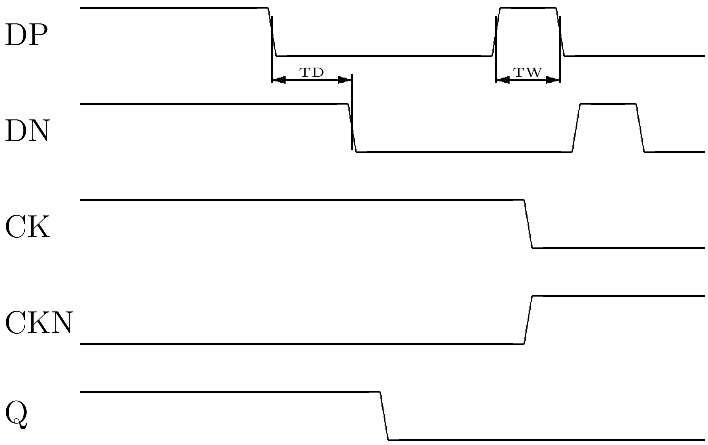

Figure 3: Transient Disturbance with Temporal Separation

The delay element is composed entirely of conventional transistors and is therefore compatible with standard commercial processes and design techniques. Furthermore, the delay time tends to track any increases in node recovery time due to environmental conditions or processing variation. This is in contrast to designs that use highly resistive polysilicon to create delay effects, where the temperature coefficient of the delay often leads to significant over design and loss of performance [13].

Having minimized the sensitivity of the latch to propagated transients, the second half of the design challenge is to optimize the combinational logic circuits so that the duration of any such transients is also minimized. As a first step, all logic gates are required to have sufficient drive strength to recover from a particle strike within some maximum time period. Second, all logic gates are designed to minimize *pulse spreading*, which can greatly magnify the duration of voltage transients as they propagate through a logic block [14,15]. Individual transistors within each logic gate cell are optimized so that the delay from any single input to the gate output is equal for both rising and falling edges. Simulations of a combinational test circuit indicate that this technique can reduce the width of the final transient at the latch input by a factor of almost four.

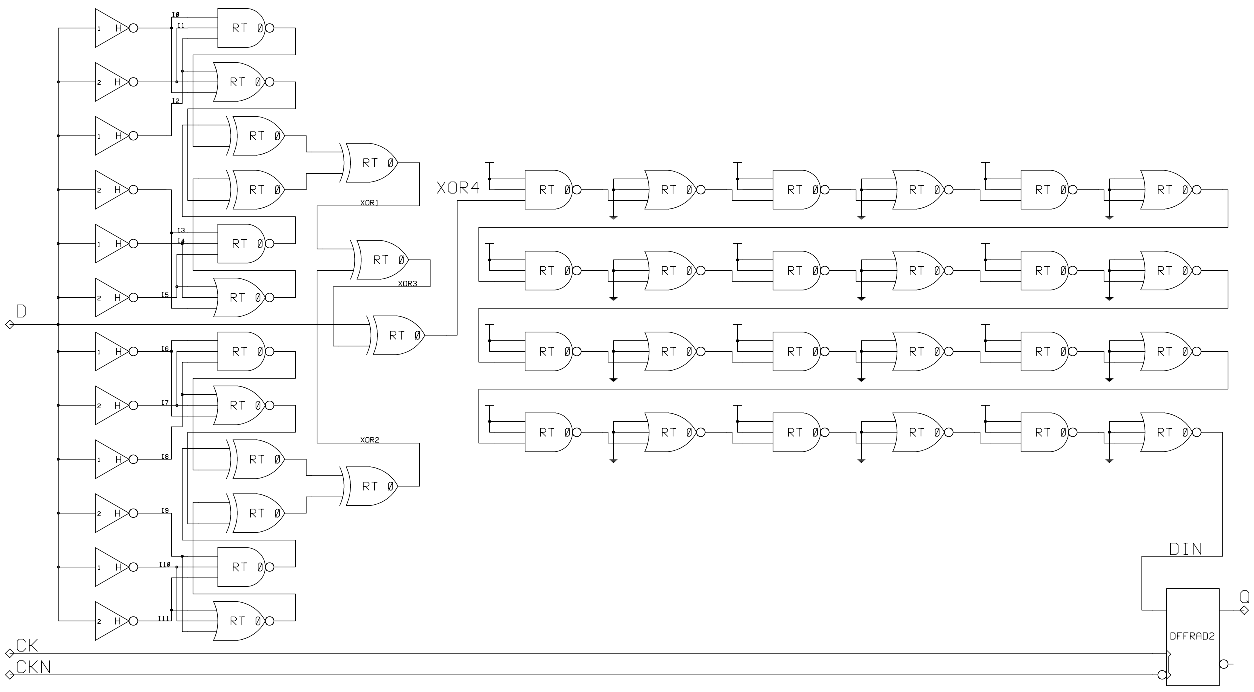

Figure 4: Combinational Logic Test Circuit

3 Test Circuits

A suite of test circuits was designed for evaluating and characterizing single-event upsets that originate in combinational logic. Each test circuit is a 32-bit shift register composed of bit cells like the one shown in Figure 4. On the left side of the schematic are twelve inverters with their inputs connected together. This common connection also serves as the data input to the register cell. The inverters are relatively weak and their drain regions have been enlarged, so they act as heavy ion or laser targets. Any pulse occurring at the output of one of these inverters will propagate through either a NAND or a NOR gate (depending upon the polarity of the D input) and then through three levels of exclusive-OR gates. The transient pulse is then combined with the D input in a final exclusive-OR gate, which has the effect of briefly inverting the value of D. The output of the exclusive-OR tree is fed into a series chain of 24 3-input NAND and NOR gates. It is this chain of gates that may produce significant pulse stretching.

The output from the NAND/NOR chain feeds the data input of the register cell's flip flop, and the Q output of the flip flop drives the data input of the next, identical cell in the shift register. The flip flop shown in Figure 4 is the radiation-tolerant standard cell flip flop, which is an edge-triggered flip flop composed of two latches (as shown in Figure 2) and a delay element between the DP and DN inputs of the master latch. This cell also provides buffered Q and QN outputs.

For characterization purposes, two different NAND/NOR chains are used. Some shift registers have gates that have been optimized to reduce pulse spreading while others have more conventional NAND/NOR gates. In the conventional gates all NMOS transistors and all PMOS transistors have the same width, which is set equal to the widest transistor in the corresponding optimized gate. Logic blocks constructed using this design style are further referred to as “gate array logic”. In addition, different flip flop styles were used in the shift registers. The three variations here were a typical non-SEU-hardened flip flop, a simple SEU-tolerant flip flop composed of two SEU-tolerant latches, and the SEU-tolerant flip flop with a delay element for temporal separation. For the SEU-tolerant flip flop without temporal separation the DP and DN inputs to the master latch were simply connected together.

4 Test Results

Single-event testing in support of the Radiation-Tolerant Standard Cell Library was conducted at the Twin Tandem Van de Graaff facility at Brookhaven National Laboratory on June 9th and June 10th, 1998. The test chip was fabricated by MOSIS in the Hewlett-Packard CMOS14 (0.5 μm) process as part of fabrication lot N7CQ. CMOS14 has previously demonstrated a high degree of total dose hardness for levels up to 300krad [16]. No latchup occurred in the radiation-tolerant cells for any Linear Energy Transfer (LET) value up to $160 MeV/mg/cm^2$ and a V_{DD} value of 3.7 volts.

In addition to the combinational logic SEU circuits, several shift registers on the test chip were used to evaluate the inherent SEU immunity of simple flip flops. The test results from these circuits verified that the radiation-tolerant flip flop discussed above is essentially immune to single-event upset for LET values up to $160 MeV/mg/cm^2$. A shift register composed of conventional, non-radiation-tolerant, flip flops exhibited SEU at an LET of $7.0 MeV/mg/cm^2$ and had a saturation cross section of about $9 \times 10^{-7} cm^2$ per flip flop.

Three different 32-bit shift registers as shown in Figure 4 were used to evaluate SEU contributions from combinational logic. The first shift register represented a conventional design style, using conventional flip flops and a gate array logic style. Another shift register consisted of radiation-tolerant standard cell flip flops separated by gate array logic. The third shift register uses radiation-tolerant standard cell flip flops with temporal separation and an optimized logic block. *Note that the first-stage inverters in the test circuits are weaker than the smallest inverter in the radiation-tolerant cell library, so the LET upset threshold is likely to be higher for a true radiation-tolerant standard cell design. The larger cells in the radiation-tolerant library will recover from single events more quickly and produce narrower voltage disturbances.*

Figure 5 shows the SEU cross section data for these three shift registers at a V_{DD} of 3.0V and a clock frequency of 32 MHz. Several important comparisons can be made from the upset cross section data on these shift registers. Note that the saturation cross section for the conventional design style is approximately twice as large as that of the flip flop cell itself, indicating that about half of the upsets in this circuit are from particle strikes to the combinational logic. It is also significant that the shift register which uses SEU immune flip flops, but does not have temporal separation or optimized logic, has a low upset threshold and a saturated cross section almost as large as the conventional design. This illustrates that upsets originating in combinational logic can be a significant contribution to the total upset rate, and can nearly eliminate the advantage of an SEU-immune flip flop. Finally, the shift register which uses temporal separation and optimized logic gates has a much higher

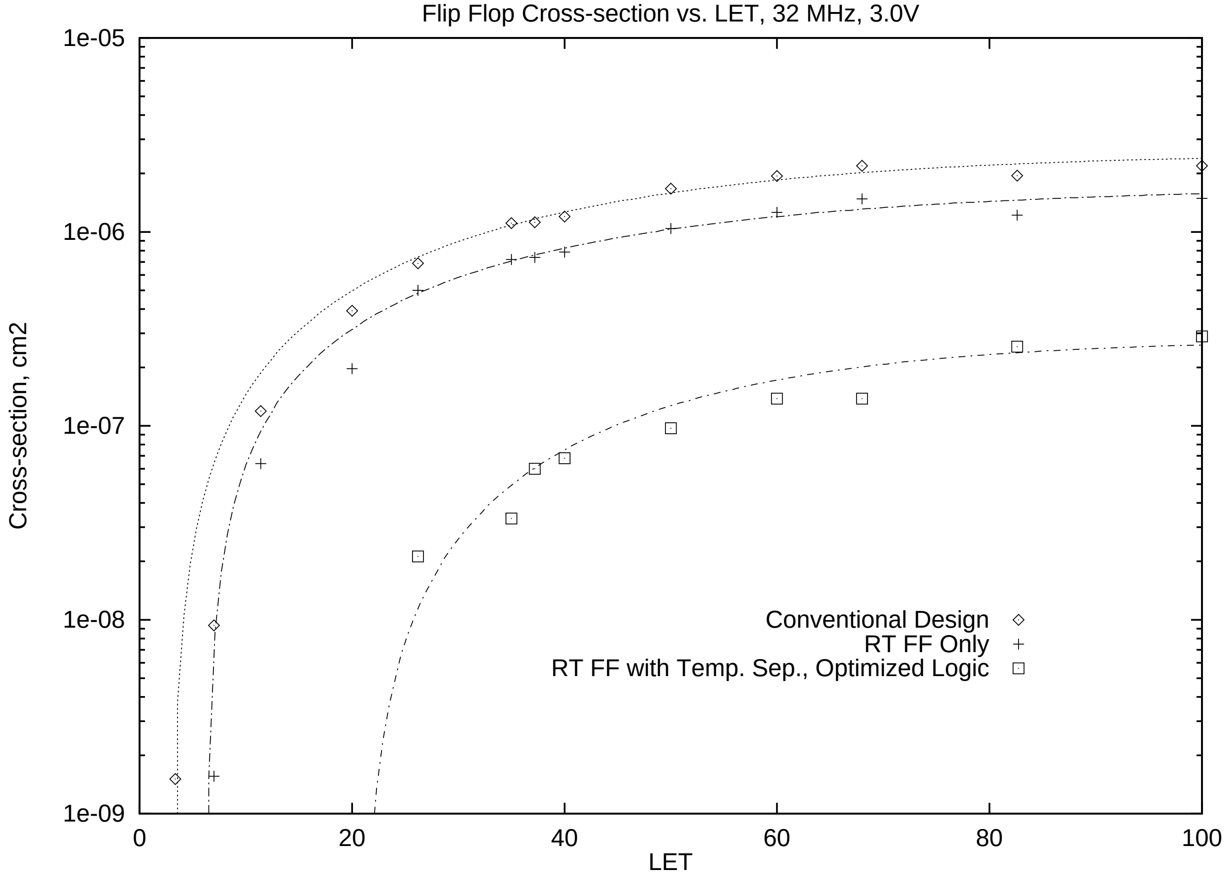

Figure 5: Combinational Logic SEU

SEU threshold and a much smaller saturated cross section. Since the probability of a cosmic particle strike decreases rapidly for LET greater than 30, the optimized design will have a greatly reduced error rate.

Figure 6 shows the relationship between clock frequency and upset cross section at an LET of 40 with a V_{DD} of 3.0V. A similar relationship was observed at an LET of 120, but the cross section areas were significantly larger. As expected, this relationship is linear with clock frequency. The test chips are capable of operation at a clock frequency of 50 MHz or more so this testing did not approach the limit of device operation. It seems likely that the relationship shown here may become non-linear, with the cross section increasing more rapidly, as the clock frequency approaches the device limit.

An important implication of this data is that SEU testing must be performed at a high clock frequency. In particular, if a device with SEU-immune flip flops is tested at a low frequency, such as 1 MHz, the true upset rate may be grossly underestimated. At the very least, testing should be done at several clock frequencies in order to characterize the relationship between frequency and upset cross section. Perhaps a new metric is needed, where the cross section is specified in cm^2/MHz to reflect the true nature of the upset mechanism.

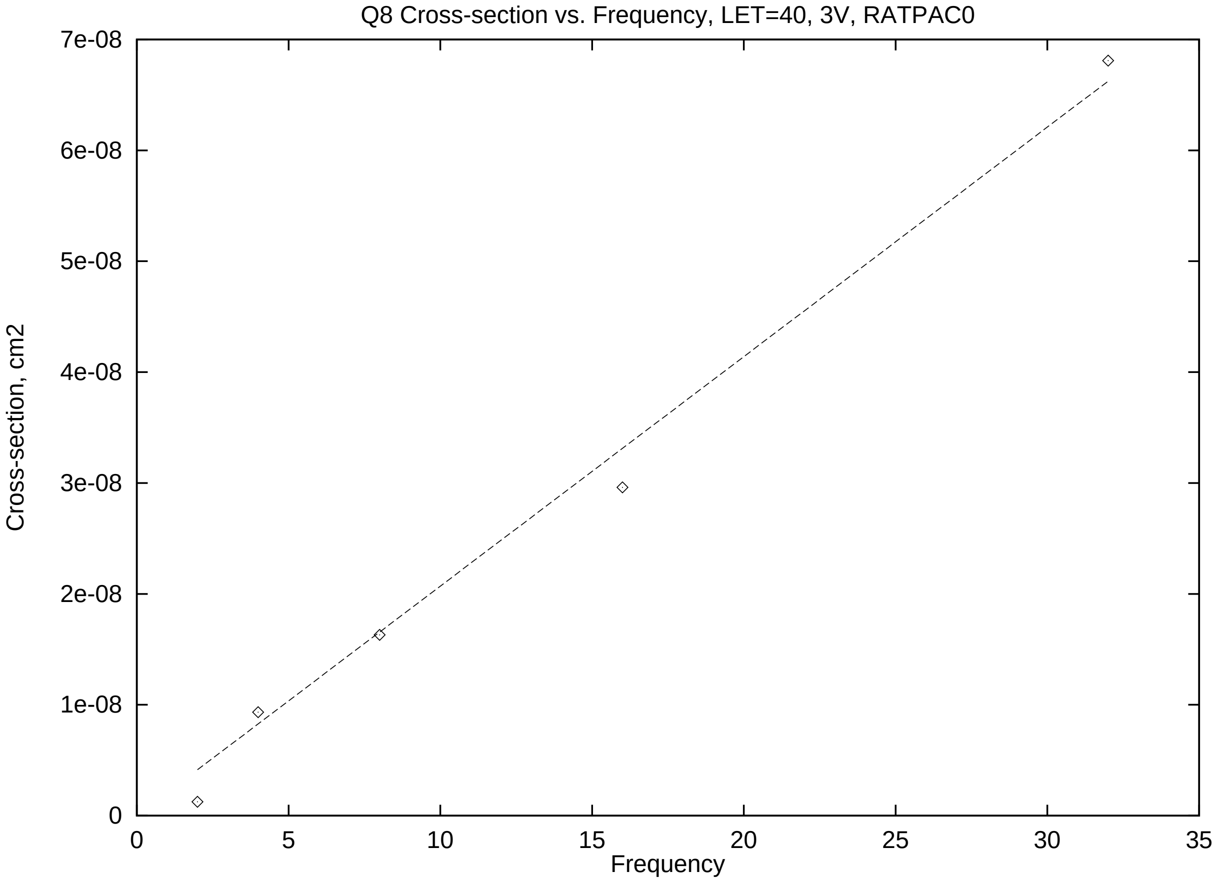

Figure 6: Combinational Logic SEU vs. Frequency

5 Summary

Single-event upsets that originate in combinational logic have been observed during heavy ion testing. These upsets can be a very significant factor in determining the actual error rate for a system, and may seriously limit the advantage of SEU-immune flip flops. SEU testing at low clock frequencies may mask this vulnerability. Techniques for mitigating the effect of SEU from combinational logic have been successfully demonstrated. These techniques are compatible with conventional integrated circuit design and manufacturing processes, and have been incorporated into a low-power, 0.5μm, standard cell library.

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