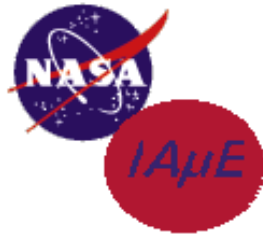


Mitigating Single Event Upsets From Combinational Logic

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SEU from Combinational Logic: What Is It?

- Cosmic particle strikes to combinational logic cause brief voltage disturbances (glitches)
- Disturbance propagates through logic gates, which may stretch the pulse width
- Glitches on DATA input during the flip flop setup time may be latched, resulting in SEU
- Glitches on CLOCK or RESET lines can upset many flip flops
- Risk increases linearly with higher clock frequencies

SEU from Combinational Logic: Why Do We Care Now?

- Voltage transients look like valid signals in fast modern technologies
- Signal line capacitances are lower, easier to disturb
- Power supply voltages are dropping, voltage transients are relatively more severe
- High clock frequencies increase probability of latching a transient
- Systems become more complex, error rate of individual components must be reduced to maintain mission success

SEU from Combinational Logic: What Do We Do About It?

- Start with SEU immune flip flops
- Design clock distribution networks carefully
- Minimize the magnitude of transient pulses in logic cells
- Minimize pulse spreading in logic blocks
- Use flip flops that ignore brief transient pulses

SEU from Combinational Logic: 0.5 μ m Flip Flop SEU Data

Output	Circuit Description
Q0	Non-radiation-tolerant flip flops
Q1	Radiation-tolerant dual-rail flip flops
Q2	Radiation-tolerant standard cell flip flops
Q3	Radiation-tolerant standard cell flip flops, local PHS generation
Q4	Radiation-tolerant standard cell flip flops, local PHS & PHM generation

Flip Flop SEU Cross Section, cm^2					
LET	Q0	Q1	Q2	Q3	Q4
3.4	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
7.0	1.25E-08	0.00E+00	0.00E+00	0.00E+00	0.00E+00
11.4	7.94E-08	0.00E+00	0.00E+00	0.00E+00	0.00E+00
20.0	1.45E-07	0.00E+00	0.00E+00	0.00E+00	0.00E+00
26.2	2.71E-07	0.00E+00	0.00E+00	0.00E+00	1.29E-08
35.0	4.45E-07	0.00E+00	0.00E+00	0.00E+00	1.59E-08
40.0	5.24E-07	0.00E+00	0.00E+00	0.00E+00	1.98E-08
50.0	6.61E-07	7.90E-10	7.90E-10	0.00E+00	5.77E-08
60.0	7.57E-07	0.00E+00	7.69E-10	1.23E-08	3.61E-08
68.0	8.43E-07	0.00E+00	7.96E-10	0.00E+00	5.17E-08

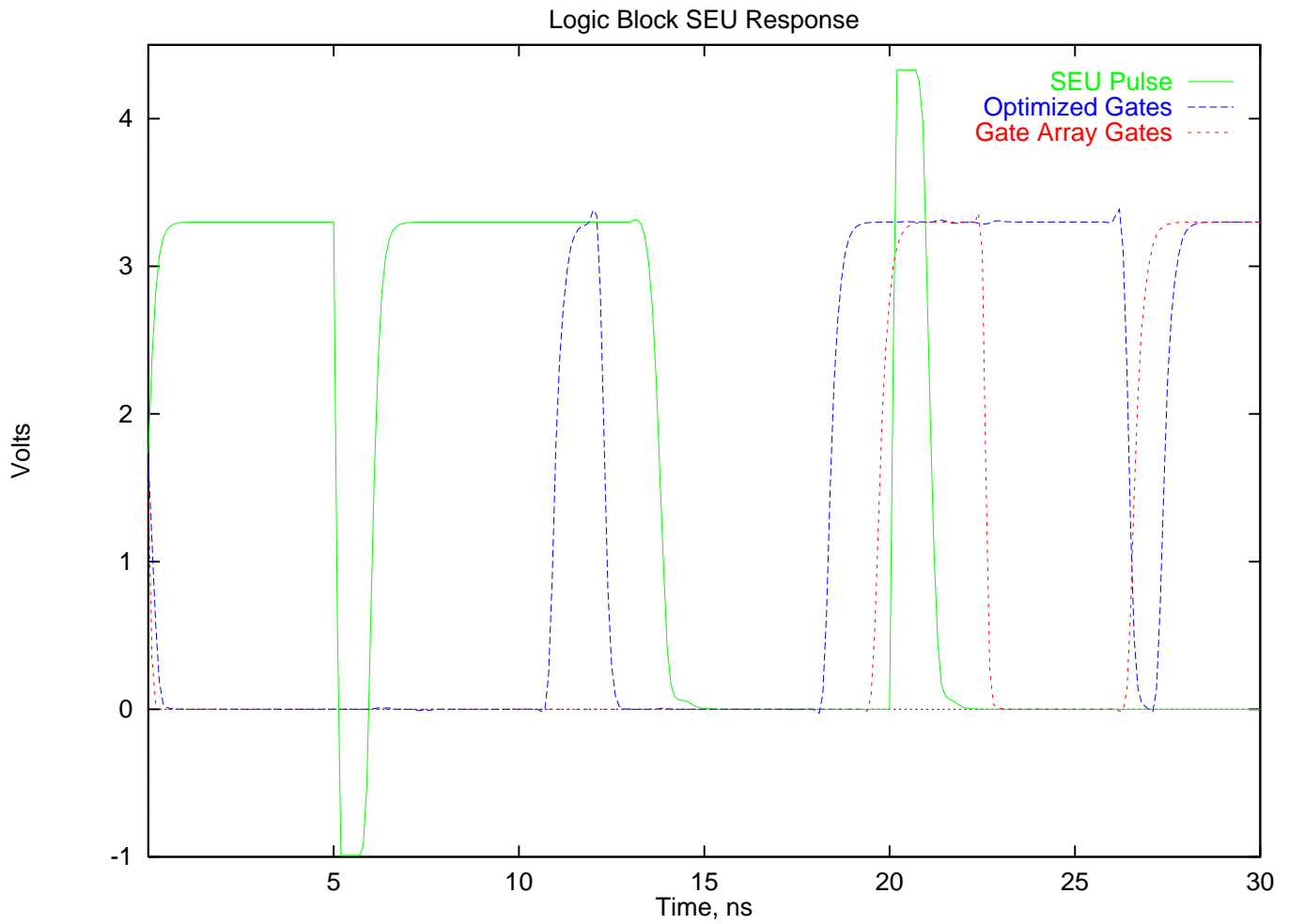
SEU from Combinational Logic: Minimizing Pulse Magnitude

- Each logic cell must meet minimum drive requirements
- Applies to internal nodes in cells as well
- Gates with high fan-in must be avoided
- Synthesis must be constrained to limit gate loading

SEU from Combinational Logic: Minimizing Pulse Spreading

- Each logic cell must be optimized
- Rise and fall delays equalized *for each input individually and for all input states*
- Avoid gate arrays with fixed transistor sizes
- New design tools may be needed to assess risk

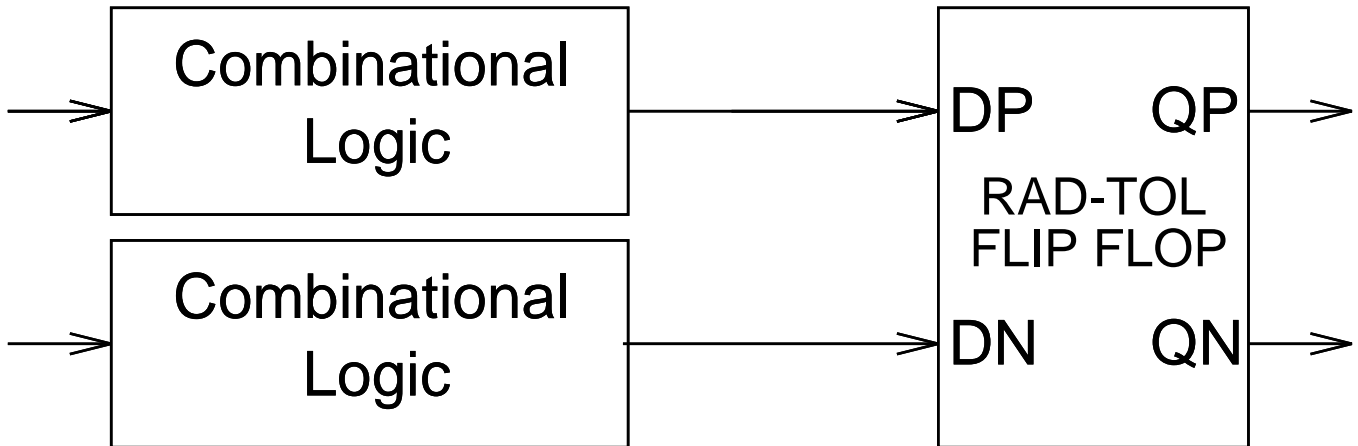
SEU from Combinational Logic: Pulse Spreading SPICE Simulation



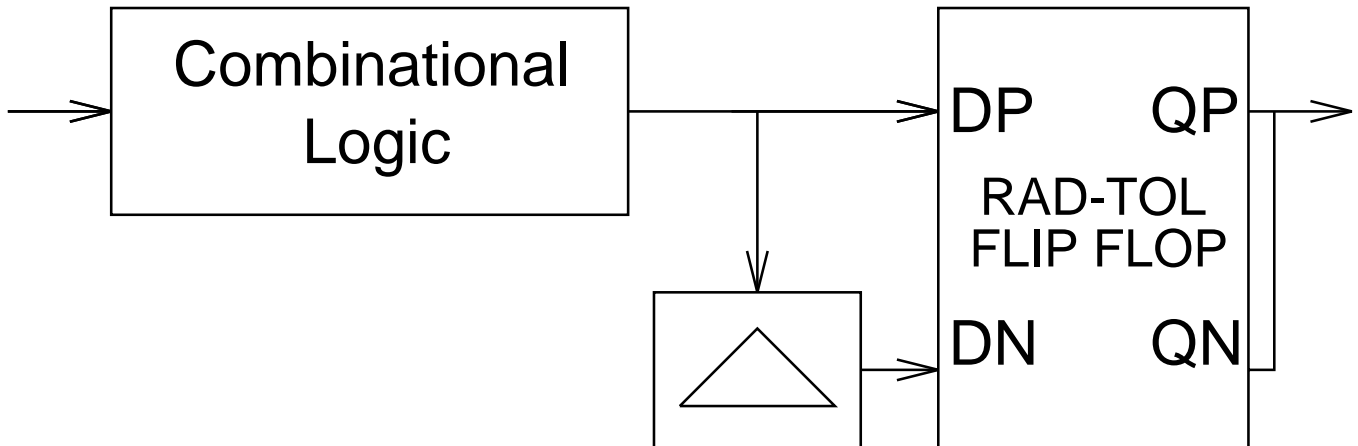
SEU from Combinational Logic: Flip Flop Design

- Design hardened flip flops must be modified
- Resistive or capacitive hardening may improve immunity
- Asynchronous SET or CLEAR should be avoided

SEU from Combinational Logic: Flip Flop Design Examples

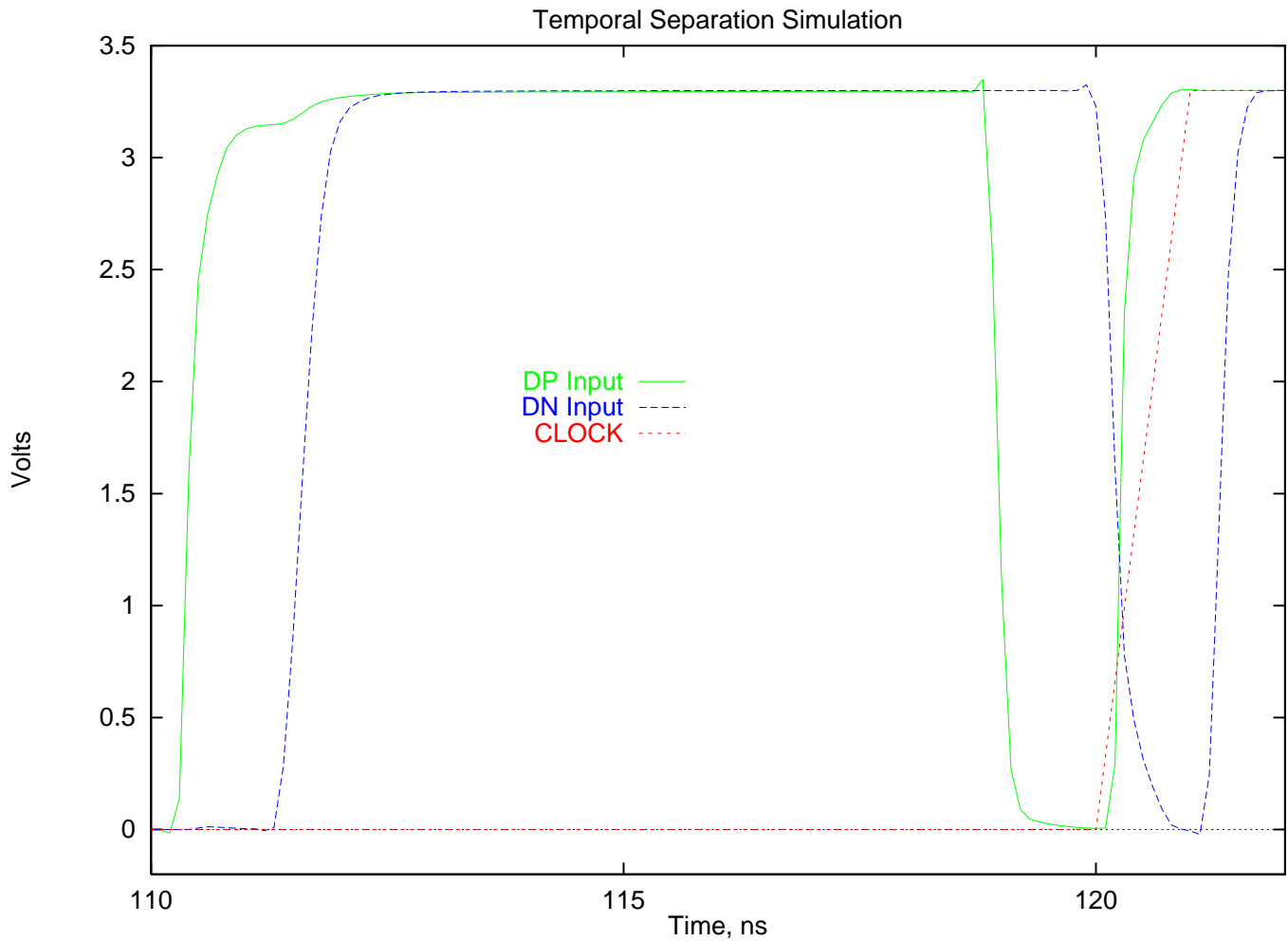


Dual-Rail Configuration

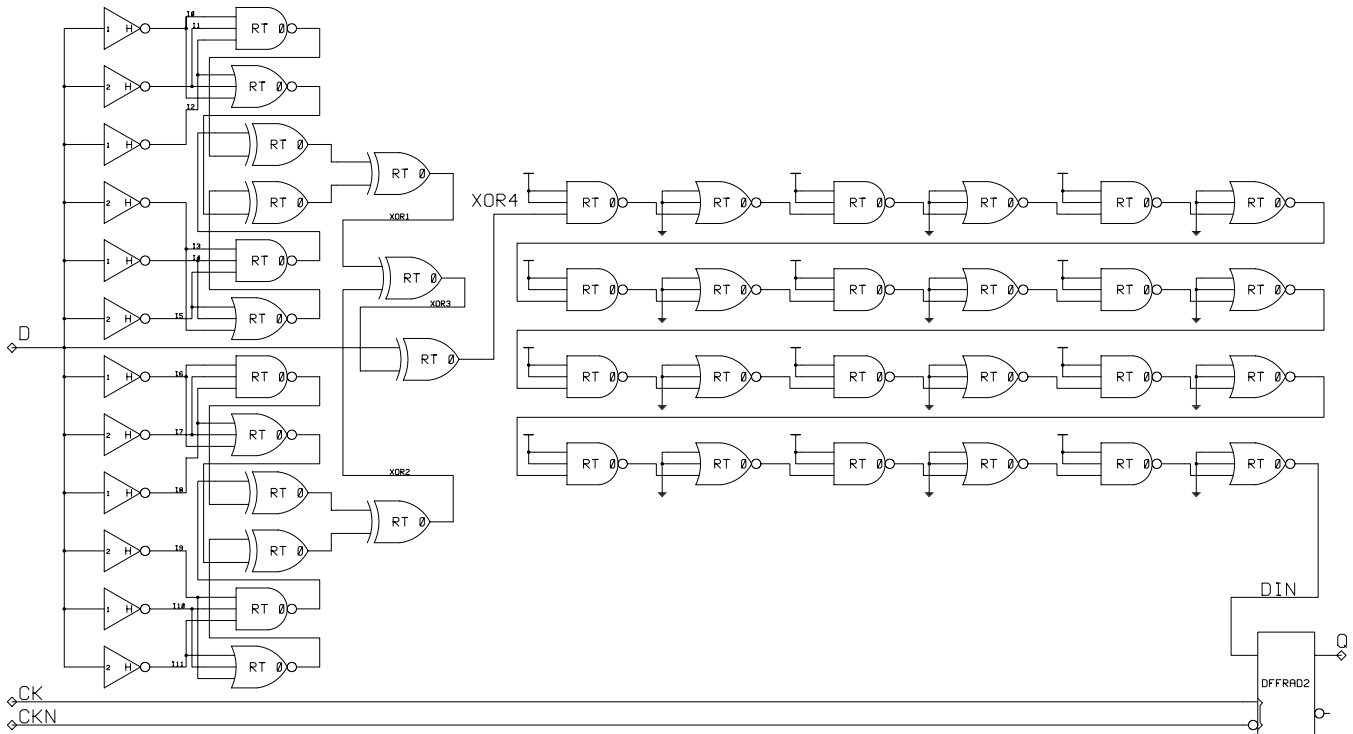


Temporal Separation Configuration

SEU from Combinational Logic: Flip Flop SPICE Simulation

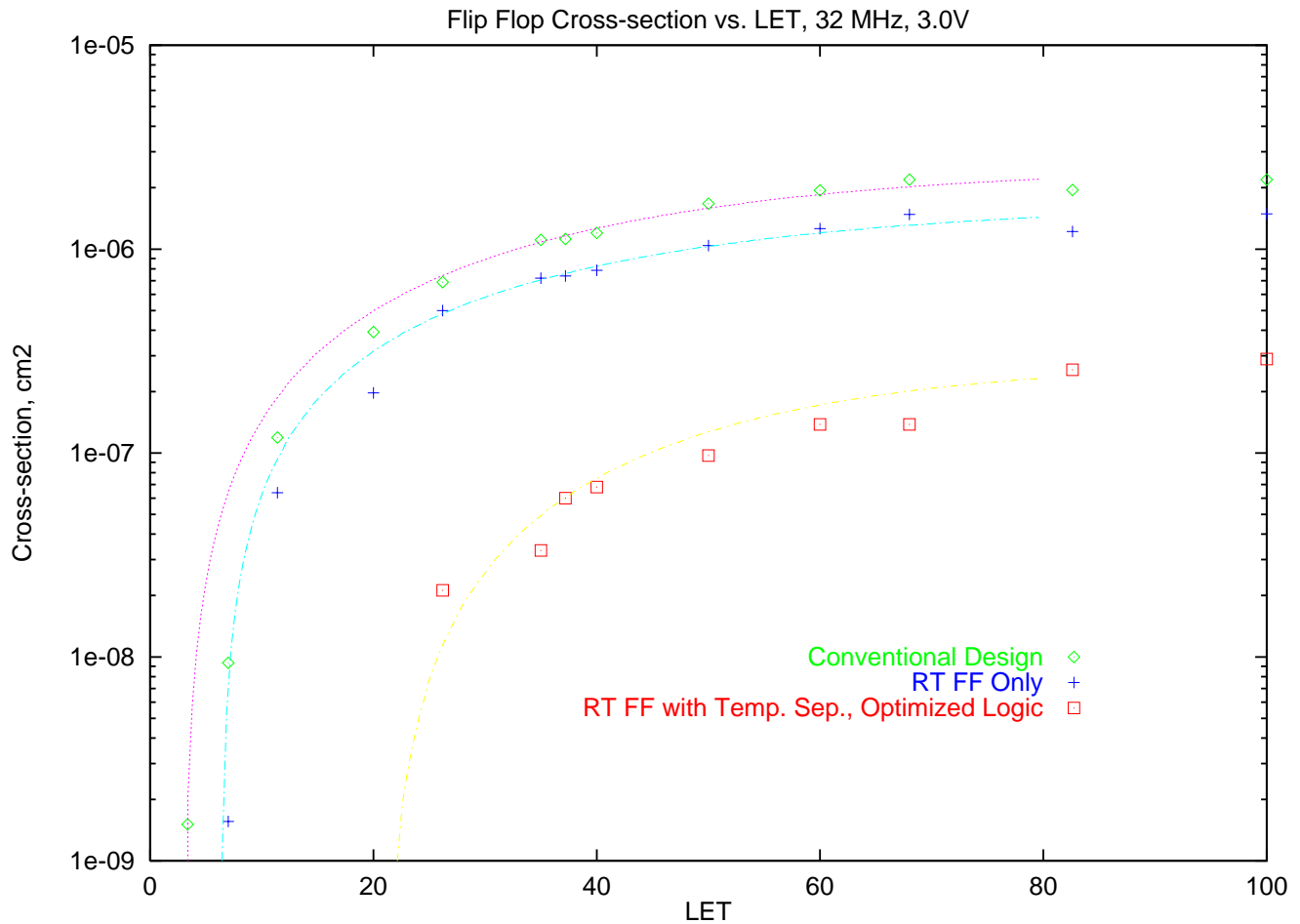


SEU from Combinational Logic: SEU Test Circuit



Output	Circuit Description
Q5	Standard cell flip flops, gate array logic block
Q6	Non-rad-tolerant flip flops, gate array logic block
Q7	Standard cell flip flops w/o separator, gate array logic block
Q8	Standard cell flip flops, optimized logic block
Q9	Standard cell flip flops w/o separator, optimized logic block

SEU from Combinational Logic: SEU Test Results



- Data for Q6, Q7, and Q8
- Curve fits are only approximate
- Results are for 0.5 μ m technology at 3.0 volts, 32 MHz

SEU from Combinational Logic: Conclusion

- SEU from Combinational Logic is a real problem
- SEU testing at low frequency may underestimate susceptibility
- Techniques to mitigate problem for MRC Radiation-Tolerant library are effective
- High levels of SEU immunity can be achieved in low-power, sub-micron CMOS