

# Probabilistic Estimates of Upset Caused by Single Event Transients <sup>1</sup>

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*Abstract* – Single event transients occur when cosmic particles strike nodes in a logic network. Transients may propagate to a flip flop and be latched, resulting in single event upset. The probability of such upsets can be estimated by considering environmental factors, circuit design parameters, and circuit usage. This procedure has been automated and used to provide qualitative evaluations of the upset vulnerability of a typical circuit. Although this technique has not yet been calibrated to actual test results it can suggest techniques for improving the upset immunity of new designs.

## 1 Introduction

Single Event Transients (SET) are an important consideration in designing modern radiation tolerant circuits. These transients occur when a cosmic particle strikes a sensitive node in a combinational logic network. The transient may propagate to the data input of a flip flop, and if it occurs near the critical setup/hold window then the transient may be stored as erroneous data. Thus the SET can have the same net result, Single Event Upset (SEU), as a direct strike to the flip flop itself [1–4].

Experiments using heavy ions have shown that SET can be a significant source of SEU, and can largely negate the benefits of using SEU-immune flip flop cells. New design techniques to mitigate the SET threat have also been demonstrated to be effective in heavy ion testing [5].

Estimating the actual upset rate for a device in any given application becomes much more difficult when the SET effect is recognized. Traditionally, the SEU rate has been estimated by considering only the likelihood that static data stored in latches and flip flops will be corrupted by a direct cosmic particle strike. These estimates ignored the dynamic behavior of the circuit and the possibility of upsets caused by SET.

## 2 Probabilistic Approach

Several earlier efforts have been made in an attempt to quantify the contribution of SET to the overall upset rate in a circuit [3, 6–8]. These researchers used a simple model for

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charge collection and simply injected fixed amounts of charge into a sensitive node, often without regard for the probability (or even possibility) that any given amount of charge collection would occur. A circuit simulation was typically performed to evaluate the transient voltage pulse that would result from injecting a fixed amount of charge, and then this voltage disturbance was introduced into a gate level logic simulation of the entire circuit to determine if a transient fault would occur. Such mixed-mode simulations do not consider that pulse stretching in logic gates varies for different inputs and input states, and can require many simulation runs to evaluate the various logic states and propagation paths in the circuit of interest.

The work described here seeks to determine the probability of upsets that originate from transients in combinational logic by examining the nature of the circuit rather than by simulating all possible event scenarios. The probabilistic analysis consists of three phases. The first analysis phase evaluates the radiation effects. Specifically, we must have an understanding of the cosmic particle environment, the orbital parameters of the spacecraft, and the physical dimensions of the circuit elements, which leads to a probability distribution for the amount of charge deposited on a sensitive circuit node.

The second analysis phase involves characterizing the logic elements used to construct a functional circuit. Each circuit element (logic gate) must then be simulated to determine the magnitude of the voltage transient that will occur as a function of the amount of charge deposited on the output node. These simulations must also consider the logic state of the circuit element and the loading present on the output node. Each circuit element is then characterized to understand how a voltage transient will propagate through it, again taking the logic state and output loading into consideration. Depending upon the relative rise and fall times for signal propagation through a circuit a transient pulse may become wider or narrower as it propagates. The latches and flip flop elements must also be characterized to determine the likelihood that a voltage transient of a given width, appearing at the data input, will be latched and cause upset.

Using this information a model of the entire combinational logic block is constructed in the third analysis phase. For each gate the probability distribution of voltage transients, as a function of their pulse width, is determined by considering direct particle strikes to the gate output as well as those transients that may originate elsewhere and propagate through the gate in question. By examining the probability distribution for transients at the flip flop data input and the characteristics of the flip flop itself we can then calculate the probability of an upset caused by SET.

## 3 Probability of Injected Charge Pulses

The first probabilistic factor to be considered is the likelihood that an SET current pulse of a given magnitude will actually occur at a circuit node. This is a difficult analysis and requires several simplifying assumptions in all but the most trivial cases [9, 10]. The natural cosmic particle environment varies greatly over time and in different orbits. A very simple approximation for the cosmic particle flux,  $\Phi(L)$ , will be used here, as shown in Figure 1 [11]. For comparison, the figure also shows a differential LET spectrum generated by the CREME96 code [12]. The units of  $\Phi(L)$  are particles per  $\text{cm}^2\text{-day}$ . The Linear Energy

Transfer, or LET, of a particle is a measure of the energy that is deposited by that particle as it passes a given distance through a material of a given density. The units for LET in the figure are MeV cm<sup>2</sup>/mg. Only particles with an LET of 30 or less are considered in this analysis, as there is actually a sharp knee in the natural spectrum at an LET of about 30 and particles with an LET above this value are exceedingly rare. By multiplying the LET of a particle by its track length in the sensitive node and by the density of silicon (2.33 g/cm<sup>3</sup>) we can determine how much energy (in MeV) will be deposited. Furthermore, each 3.6 MeV of energy will release an electron-hole pair in silicon, so the LET of a particle can be directly translated into an equivalent charge deposition.

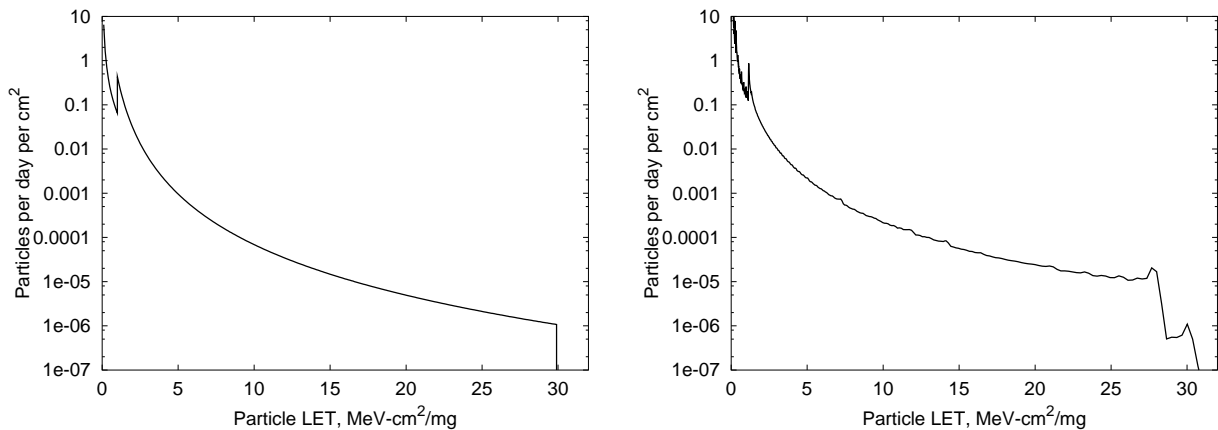


Figure 1: Differential energy loss spectrum,  $\Phi(L)$ , approximated and CREME

In the natural space environment a particle may strike a circuit node at any angle and enter at any point on the surface, leading to a distribution of possible track lengths  $S(l)$ . The sensitive volume of the circuit node is typically modeled as a rectangular parallelepiped (RPP), as shown in Figure 2. A particle entering at one corner and exiting through the farthest opposite corner traverses the maximum path length of  $S_{max} = \sqrt{x^2 + y^2 + z^2}$  while a particle that just grazes one corner has a minimum track length,  $S_{min} = 0$ . Calculating the probability density function for the path lengths through an RPP is fairly difficult, so the approximation used in [11] is also used here. This approximated integral path length distribution is shown in Figure 2 for an RPP that is 0.3  $\mu\text{m}$  thick, 1.0  $\mu\text{m}$  wide, and 5.0  $\mu\text{m}$  long.

In addition, the cosmic particle distorts the depletion region and increases the effective path length in a process called *funneling* [13,14]. As a rough estimate of the funneling effect we assume that the effective path length is 2  $\mu\text{m}$  longer than the geometric path length through the RPP and increase the values in  $S(l)$  accordingly. With these approximations we can express the probability of a charge pulse (in events per day) as a function of the injected charge (in pC):

$$P(q) = (\bar{A}_p \times (\Phi(L) * S(l)) \times \rho_{Si}) / 22.5$$

where  $*$  represents convolution,  $\bar{A}_p$  is the average projected area of the RPP,  $\bar{A}_p = (xy + yz + xz)/2$ ,  $\rho_{Si}$  is the density of silicon and 22.5 is the conversion factor from MeV to pC for

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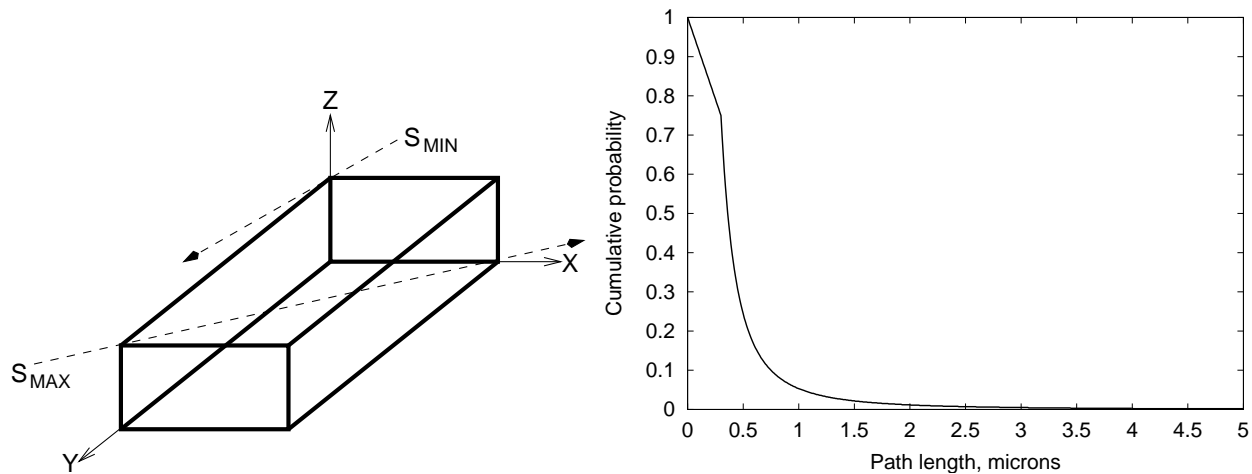


Figure 2: RPP model and integral distribution of path lengths,  $S(l)$

energy deposited in silicon. For the example RPP discussed above this function is shown in Figure 3.

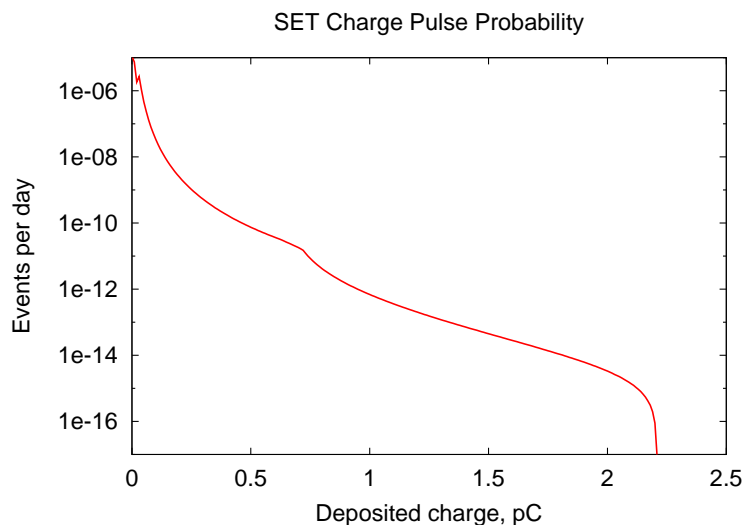


Figure 3: Probability of SET charge pulse

## 4 Behavior of Logic Elements

Digital circuits typically consist of a number of individual logic cells, or gates, that are interconnected to perform a particular function. In order to analyze the probability of an upset in the circuit, each of the cells must be characterized to determine its response to single events. This characterization takes two forms, both of which are accomplished with a circuit simulator such as SPICE. First, charge pulses of fixed amplitude are injected at

the cell's output node and the width of the resulting voltage disturbance is measured. This simulation is repeated for each of the  $2^N$  possible states of an  $N$ -input gate and over the range of injected charge pulses that the cell may experience. Unfortunately, the true response of a circuit node to a cosmic particle strike is difficult to quantify and this step may represent the largest source of error. Second, narrow voltage pulses are presented at each of the cell inputs and the width of the resulting output pulse is measured. The difference between the width of the input and output pulses is used as a fixed pulse stretching parameter, although future work will incorporate a model for the nonlinear relationship between input pulse width and output pulse width. The simulation is repeated for each cell input and for all possible states of the other (static) inputs.

The flip flop cells must also be characterized, but in this case we need to determine the likelihood that an SET error pulse appearing at the cell's data input will be latched. These simulations utilize error pulses of varying width and the leading edge of the pulse is moved with respect to the clock edge. The result is a measurement of the "latching window", during which an erroneous pulse will be latched, as a function of the width of the latch pulse. Typical results for the conventional and hardened flip flops are shown in Figure 4. Note that the latching window is different for low and high pulses. These functions are modeled as piecewise linear functions with two breakpoints.

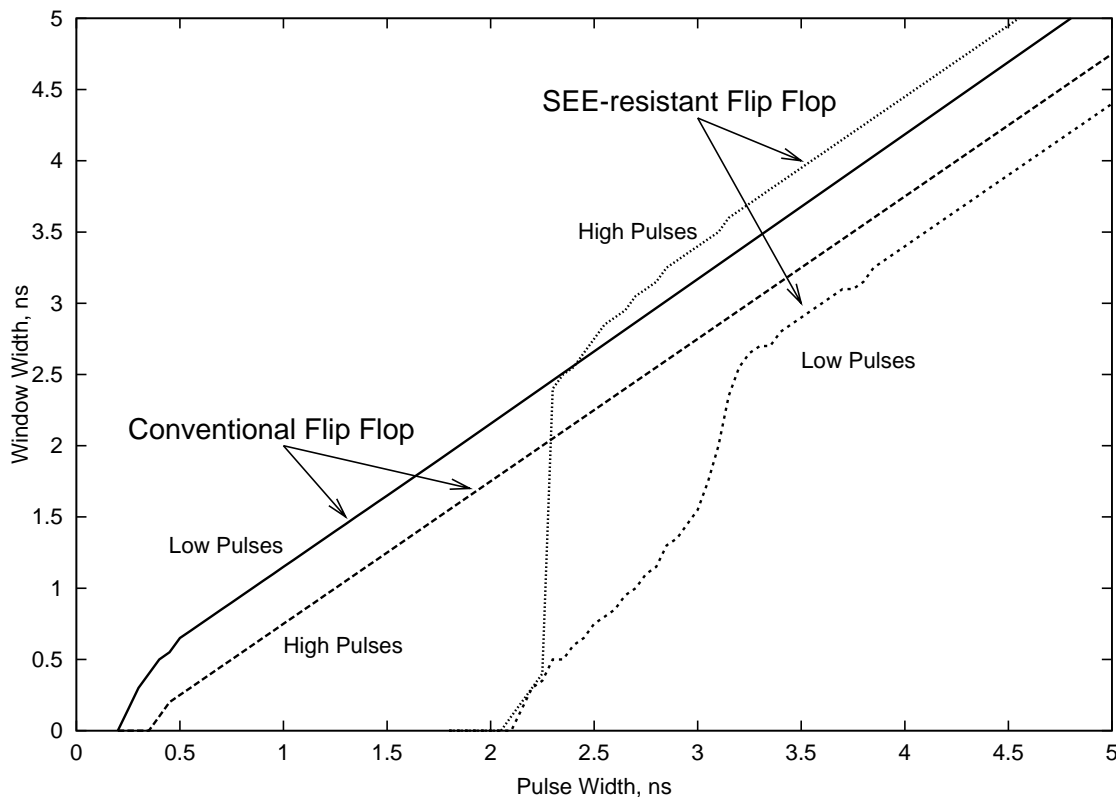


Figure 4: Flip Flop Pulse Latching Window

## 5 Probability of Latched SET

Having characterized the radiation environment and the library of logic cells, we can analyze the probability of single-event upsets caused by SET. A recursive algorithm is first used to determine the probability distribution of SET voltage pulses at the data input of each flip flop as a function of the width of the pulse. The algorithm begins by identifying the logic cell that directly drives the flip flop's data input. The probability density for pulses at this cell's output node is the accumulation of the probability density of pulses caused by direct hits to the cell's output and the probability density of pulses that can propagate through the cell, with a possible change in width, from its input pins. To determine the probability density for pulses at the cell inputs we must first identify the cells that drive those inputs and compute the probability density of pulses for the outputs of those cells. This step repeats, moving back from the flip flop's data input along all possible paths, until either a primary input or a flip flop output is encountered. A primary input experiences no SET pulses, while a flip flop can have SET pulses on its output but will not propagate pulses that appear at its input. The core of this algorithm is expressed in the pseudocode below.

```

sub pulse_prob( cell_reference ) {
  Pcell(t) = 0 # clear cell pulse probability density function
  if ( cell_reference is a primary input ) then return
  foreach ( of 2^N input states ) {
    Temp(t) = Poutput(t) in this state
    foreach ( input that is sensitive in this state ) {
      Pinput(t) = pulse_prob( the_gate_driving_this_input )
      adjust Pinput(t) by amount of pulse stretching through this input
      Temp(t) += Pinput(t)
    }
    Temp(t) *= probability that cell is in this state
    Pcell(t) += Temp(t)
  }
}

```

The result,  $P_{cell}(t)$ , expresses the number of events per day as a function of the width of the voltage disturbance that appears at the flip flop's data input. The final step is to calculate the probability that these pulses will be latched and cause an upset. The flip flop has been characterized to determine the size of the latching window for pulses of various widths,  $W_{latch}(t)$ , and we assume that SET pulses are randomly distributed in time, so the probability that a pulse of a certain width will be latched is just the width of the corresponding latching window divided by the clock period. As observed in heavy ion testing, the upset rate from SET is directly proportional to the clock frequency. The overall upset rate for the flip flop is simply the integral of this relationship over the range of possible SET pulse widths:

$$\text{Upset Rate} = 1/t_{CLK} \int_t P_{cell}(t) W_{latch}(t) dt$$

## 6 Analysis Results

This analysis was performed on a sample circuit. This circuit was synthesized from a VHDL behavioral description of a three bit adder and included an ‘all ones’ detector for the output bits (Figure 5). Each output is assumed to drive the data input of a flip flop. The table below illustrates the kind of design information that can be obtained by performing the probabilistic analysis described above. Note that the upset rate values have been normalized, as the intent at this time is to show qualitative differences.

The circuit netlist can be modified to evaluate various design changes and reanalyzed in a matter of seconds. The first entry in the table is for the circuit as shown in Figure 5, using relatively weak inverters and a poorly designed NAND gate for U14. All of the possible input states for each gate are assumed to be equally likely. The upset probabilities shown for the four outputs assume that each is fed to the data input of the conventional flip flop, as shown in Figure 4. The second and third table entries show the effect of changing the

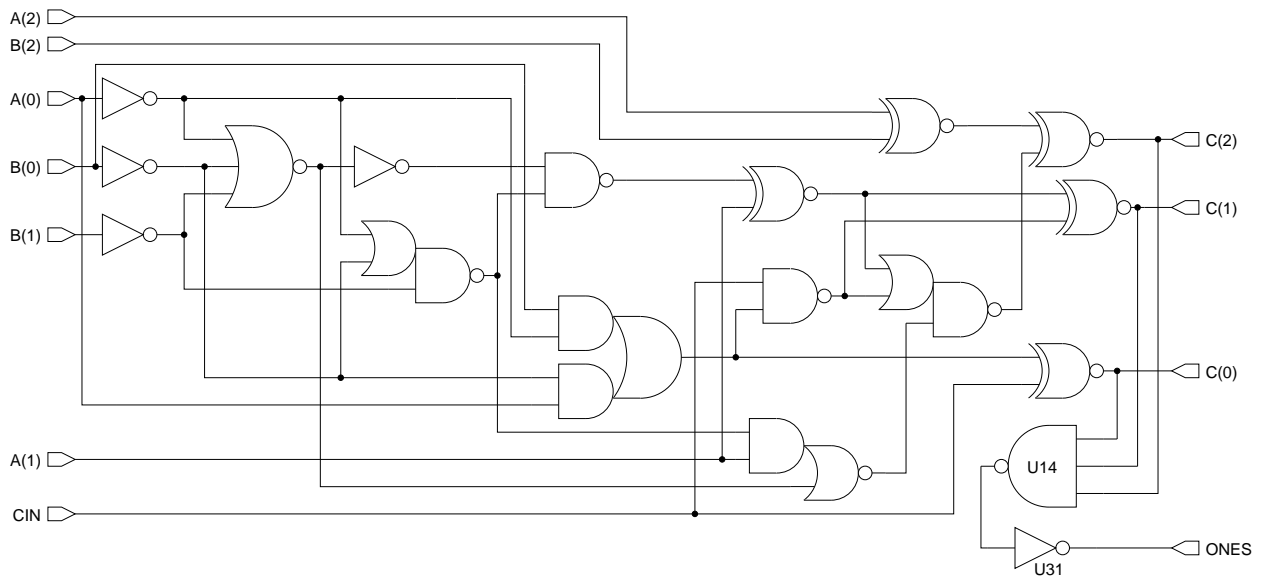


Figure 5: Three Bit Adder Test Circuit

default probability of the input states. In the second entry the probability of CIN being low has been set to 1.0, and the upset probability for output nodes C(0) and C(1) has decreased somewhat. In the third entry the CIN, A(0), A(1), and A(2) entries have a 1.0 probability of being high, as would be the case if the adder were being used to find the 2’s complement of the B inputs. In this case the upset probability for C(0) has increased significantly, with lesser increases for the other outputs.

Test Circuit	Node Upset Probability			
	C(0)	C(1)	C(2)	ONES
Original Adder	0.83	0.70	0.78	1.00
CIN always low	0.71	0.66	0.78	1.00
CIN, A(2:0) always high	0.99	0.79	0.85	1.02
Replace U14	0.83	0.70	0.78	0.91
Replace U31	0.83	0.70	0.78	0.38
Replace U14 and U31	0.83	0.70	0.78	0.29
Replace U14, all inverters	0.70	0.59	0.73	0.28

The last four entries in the table show the effect of replacing various gates with more robust equivalents. The 3-input NAND gate, U14, in the ONES output path was replaced with a gate that had been optimized to reduce pulse spreading, which decreased the upset probability for ONES by about 10%. Replacing U31, the inverter that drives the ONES output, with a stronger inverter reduced the upset rate for this output by over 60%, suggesting that most of the upsets at this node are due to direct hits to this inverter's output rather than pulses that propagate through the logic network. Replacing both U14 and U31 reduces the upset rate on ONES by over 70%. Finally, replacing U14 and all of the inverters improves the upset rate for all outputs as shown in the last line of the table.

## 7 Conclusion

A general technique for evaluating the probability of single event upset due to transients in combinational logic has been described. This method has been implemented in software and applied to an example circuit. The analysis results provide a relative evaluation of different circuit variations. Ongoing efforts will improve the models for injected currents and pulse stretching, and will attempt to correlate the upset rate predicted by this tool to the observed error cross section of actual devices tested with a heavy ion beam.

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