

Symmetrical Subranging R2R DAC in ULP

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Abstract – An 8-bit R2R DAC structure is derived that is able to produce 255 steps over any subrange of the normal R2R reference voltage with the center of the range coinciding with the center of the reference range and with the subranging being achieved without the use of active attenuators having to be added to an R2R structure. An example is given with an application in the ULP process. The DAC reference range is .5 volts, which is the same as the VDD for the ULP process. An example DAC range of .2 volts to .3 volts is given as an example.

1. Introduction

CMOS DAC's have commonly been done by switching CMOS current sources on or off into a common node [1]. The current sources are weighted by using device widths that increase as a power of two for increasing binary-valued current sources that are turned on by the corresponding binary bit in the input word. The common output node can be used directly. In that case the DAC is a current DAC. Or the output node can drive an opamp with a resistive feedback element. In that case the output is taken on the output node of the opamp and is a voltage. A simple block diagram of an eight-bit DAC is shown in Figure 1.

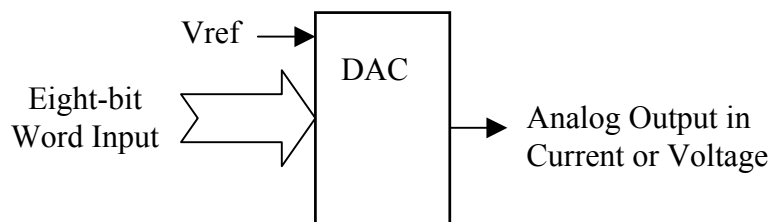


Figure 1. Simple DAC symbol.

Ultra Low Power structures use CMOS devices at very low voltages. A VDD of .5 volts is typical for ULP designs. These devices tend to have higher static current leakages than regular CMOS devices that are designed to operate at 2 volts or higher. These static leakages could corrupt the current conversion process if used in the DAC structure. The output of the DAC in Figure 1 is given by equation (1). The eight-bit digital word is given by the coefficients d_i and the value is found by multiplying the coefficient d_i (0 or 1) by its corresponding column value of 2^i and then adding all the non-zero column values.

$$V_{out} = V_{ref} * D / 2^8 = V_{ref} * (d_7 2^7 + d_6 2^6 + \dots + d_1 2^1 + d_0) / 2^8 \quad (1)$$

If V_{ref} is assumed to be VDD the DAC output will range from 0 volts to $VDD * (255/266)$, depending on the value of the digital word $D = d_7 d_6 \dots d_1 d_0$.

2. R2R DAC's

The R2R structure has been used to create Digital-to-Analog Converters (DAC's) in the lower resolution range (up to ten bits) for years [1 - 5]. The typical structure is shown in Figure 2. The R2R resistive network is used as a binary controlled current source that injects current into the virtual-ground node of an opamp which is then forced through the feedback resistor to give an output voltage. A few of the drawbacks of this structure are the necessity of generating a low-offset gain element (opamp) as well as requiring a negative output voltage range. The output range limits are specified by the V_{ref} and Ground voltages, as well as the feedback resistor value.

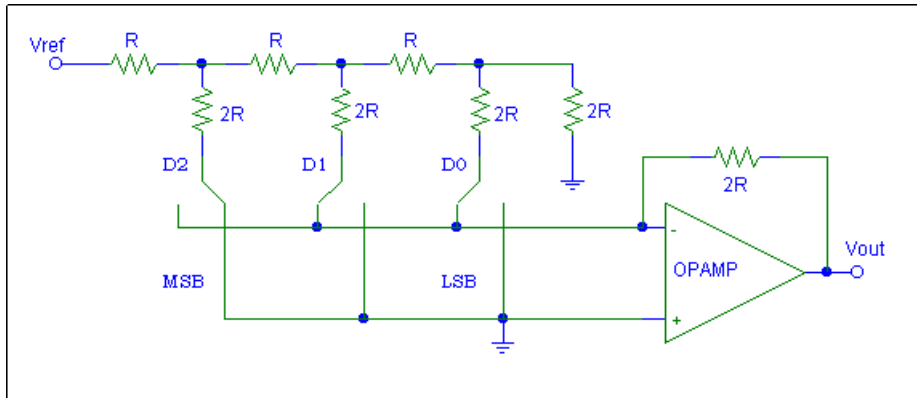


Figure 2. R2R DAC with voltage output.

The output voltage of the DAC in Figure 2 can be found from the product of the current forced into the virtual ground node of the opamp and the feedback resistor [4].

$$V_{out} = -2R * I_{TOT} \quad (2)$$

Where ITOT is the total current from the R2R structure into the virtual ground node. With the switches as shown in Figure 2, and noting that the switches terminate in Ground in either of their positions, the output could then be found by noting that each node in the R2R structure is one-half the value of the node to the left, as given in equation (3).

$$\begin{aligned} V_{out} &= -2R \cdot V_{ref} \cdot (0 \cdot .5 + 1 \cdot .25 + 1 \cdot .125) / 2R \\ &= -.375 \cdot V_{ref} \end{aligned} \quad (3)$$

Both positive and negative supplies are needed for this type of R2R DAC structure.

2. R2R Voltage Output Structure

The R2R structure itself can be analyzed in a voltage mode to provide a voltage output directly. Figure 3 shows the Thevenin equivalent structure that results from decomposing the switches and the rails they tie to. The first Thevenin equivalent circuit is seen from inspection to be given

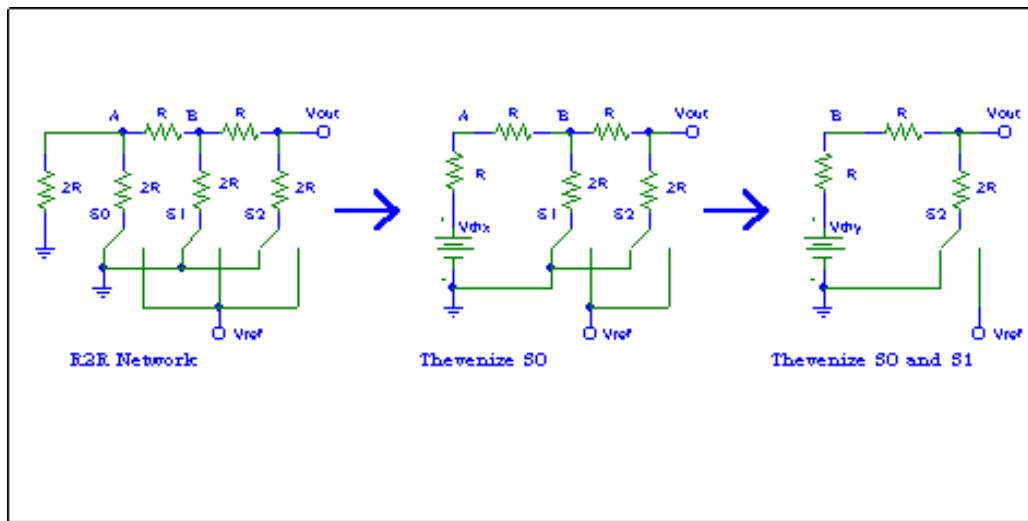


Figure 4. Steps to Thevenize R2R network.

by equation (4). The Thevenin voltage, V_{thx} , is generated from the two leftmost “2R” resistors and the voltage switch between zero volts and V_{ref} . The coefficient d_0 accounts for the switch S_0 being tied to Ground or V_{ref} . If S_0 is tied to Ground d_0 equals zero, otherwise it is equal to “1”.

$$V_{thx} = d_0 \cdot V_{ref} / 2. \quad (4)$$

Similarly, the Thevenin voltage V_{thy} can be found by combining the voltage from S_1 and the Thevenin voltage V_{thx} . Simple analysis gives the result in equation (5).

$$V_{thy} = V_{ref} \cdot (d_0 / 4 + d_1 / 2), \quad (5)$$

Where d_0 and d_1 are the coefficients controlled by S_0 and S_1 respectively (zero if tied to Ground and “one” if tied to V_{ref}). Note that if all the R2R elements are Thevenized in a network, the final Thevenin voltage would be the output voltage of the DAC that has an output impedance of R . This analysis can be extended to any number of R-2R elements. For example, an eight-bit R2R voltage DAC would have its output given by equation (6).

$$V_{out} = V_{ref} * (d_0/256 + d_1/128 + \dots + d_6/4 + d_7/2). \quad (6)$$

Or, equivalently:

$$V_{out} = V_{ref} * (d_0 + d_1 2^1 + \dots + d_6 2^6 + d_7 2^7) / 2^8, \quad (7)$$

which is seen to be identical to equation (1). It can be noted that the DAC range will go from Ground to $V_{ref}(1 - 1/2^8)$ if the leftmost 2R resistor is tied to Ground (as shown in the example), or it will go from $V_{ref}/2^8$ to V_{ref} if the leftmost 2R resistor is returned to V_{ref} .

3. A Subranging R2R DAC

We can modify the Thevenin equivalent sources in each of the R2R legs to provide voltages other than Ground and V_{ref} (or VDD) by using resistor voltage dividers and switching each side of the resulting divider. A single element of the R2R structure is shown in figure (5). The switching elements are logic values provided by the logic signal and its inverse. The logic values in a CMOS circuit are VDD and Ground. The resistance added by the CMOS conducting element (either a PMOS or NMOS device) adds a small amount of resistance to the 2R resistor. To keep the ratio between the 2R element and the R element equal to two a small amount of resistance equal to a fraction of the resistance of the “on” CMOS device can be added to the R element. The PMOS and NMOS devices can be sized to give equal “on” resistances in the non-saturation mode (triode mode) of operation [5].

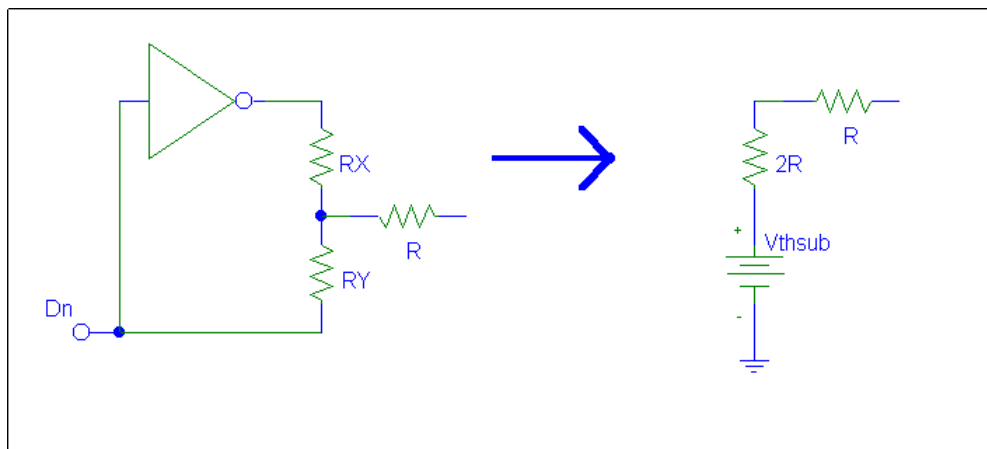


Figure 5. Means to Develop a Subranging Element in an R2R DAC.

The RX and RY resistor values are chosen to generate the maximum and minimum voltages that will appear on the output of the DAC. The Thevenin equivalent max or min voltage is determined by the logic level (and hence voltage) of Dn. The parallel combination of RX and RY will also have to have an equivalent resistance equal to 2R.

A subranging DAC has been designed for the ULP (Ultra Low Power) process developed at the Microelectronics Research Center at the University of New Mexico with the DAC output requiring 255 voltage steps between .2 volts and .3 volts. The VDD of the ULP circuit was .5 volts. Figure 6 gives the R2R schematic and Figure 7 shows the simulated output results.

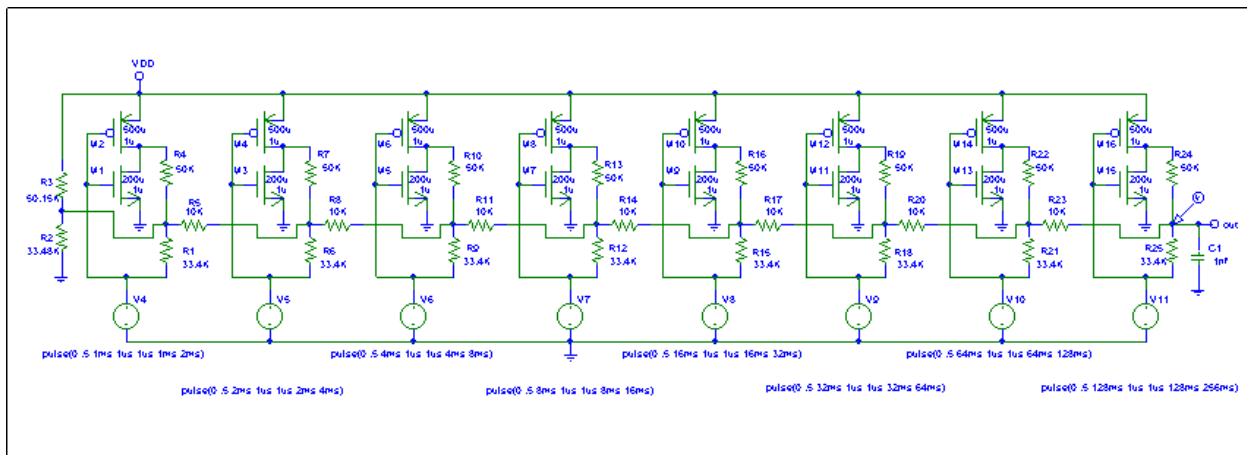


Figure 6. 8-bit R2R Subranging DAC with .1 volt range.

An equivalent leftmost “2R” element has to be included in the resistor chain as shown in Figure 6. This divider provides a Thevenin equivalent voltage of .2 volts (the minimum voltage in the DAC range) and the parallel combination of the 50.15K and 33.48K give a 2R value of 20K. Voltage sources provide the logic and timing necessary for the simulation step output shown in Figure 7.

The glitches in the DAC output simulation are due to the transients in the switching and are not error levels in the DAC itself. The output model for this DAC would be a voltage source in series with a 10K resistor.

4. Conclusions

The classic R2R structure that has been used in DAC’s for years has been modified to give a subranging voltage output. No active analog devices are needed to provide a usable output and the control structure consists of simple logic gates. The DAC example used in this paper could also be used with a resistive feedback opamp to provide a selectable gain or attenuation. The opamp would also be able to operate within a single supply environment since its output would not necessarily have to go negative (below Ground) as required in the normal R2R structure.



Figure 7. Subranging R2R DAC Simulation Results.

References

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