

Single Event Transients In Deep Submicron CMOS

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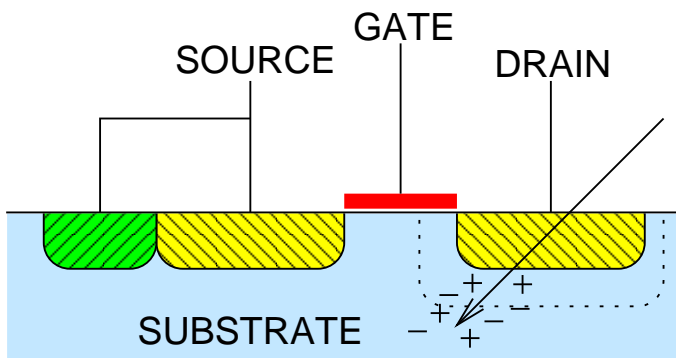
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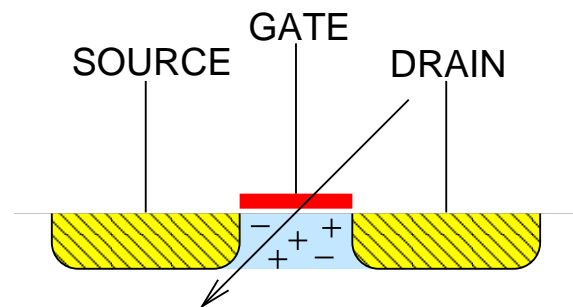
Single Event Transients In Deep Submicron CMOS

- Source of Single Event Transients (SET)
- Mechanism for Single Event Upset (SEU) caused by SET
- Impact of logic circuit design
- Experimental results from heavy ion testing
- Design considerations for single event tolerant systems

Source of Single Event Transients



BULK CMOS

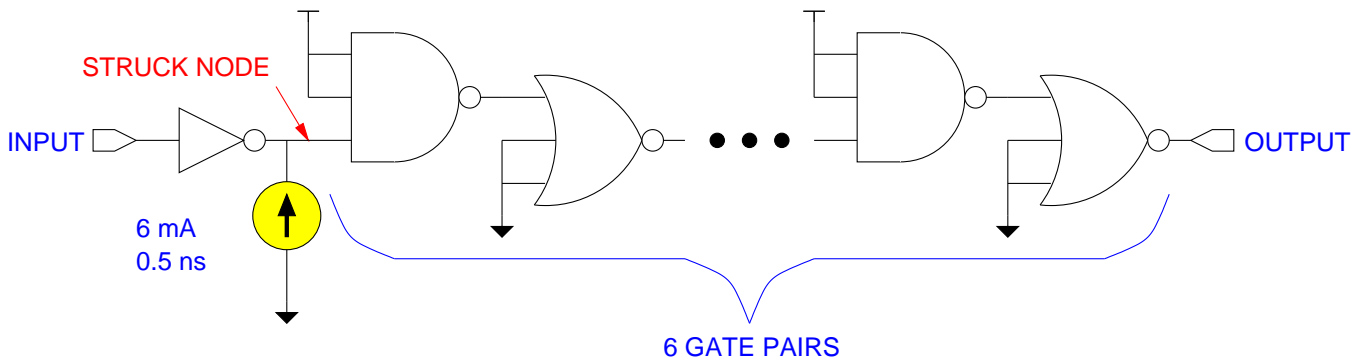


SOI CMOS

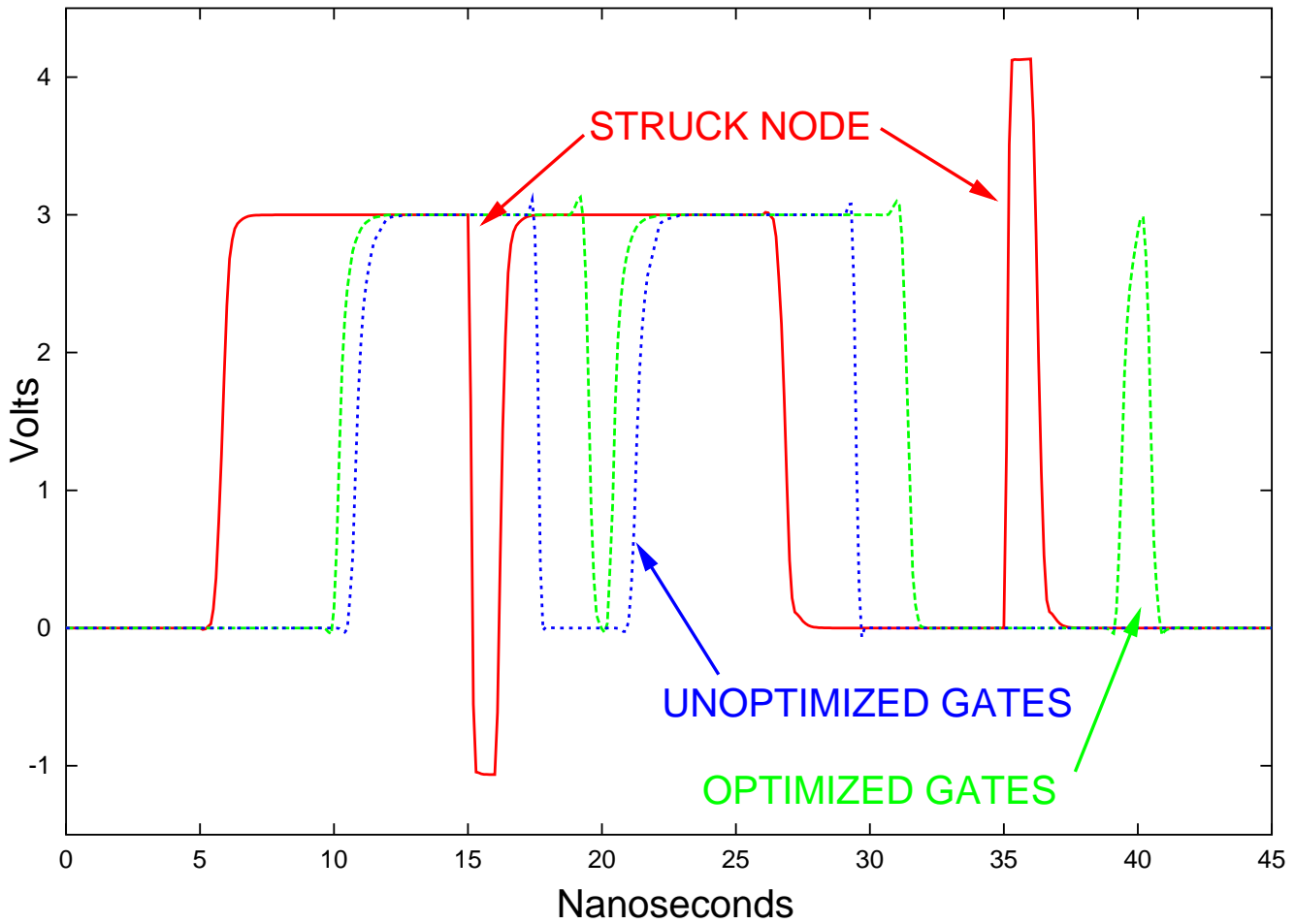
- Energetic subatomic particle from space or packaging material passes through transistor
- Particle creates electron-hole pairs
- In bulk CMOS, field in depletion region separates carriers
- In SOI CMOS, parasitic bipolar can be triggered
- Net effect is to inject charge and cause the voltage at a circuit node to change
- Quantitative analysis/simulation is difficult

Mechanism for SEU caused by SET

- Voltage transients within a flip-flop can change its state
- Transients on clock or reset lines cause global changes
- Transients propagating to flip-flop data inputs can be latched



Impact of Logic Circuit Design



- Voltage transients exceed V_{DD} and V_{SS} at struck node, greater impact at low supply voltages
- Conventional logic (unoptimized) stretches pulses of one polarity, shrinks pulses of other polarity
- Optimized logic preserves pulse width

Experimental Results

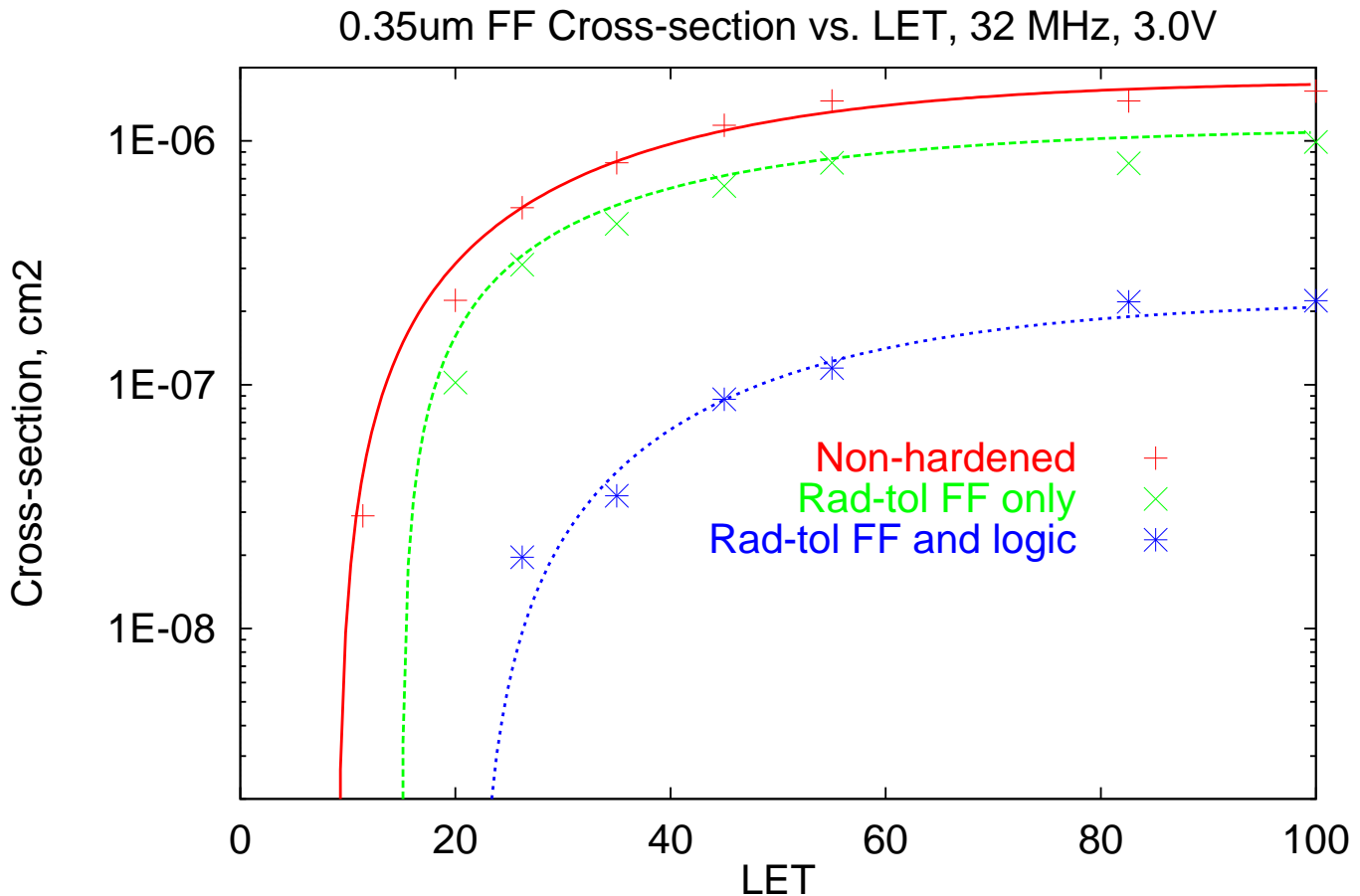
Flip-flop Data

0.35 μ m Flip Flop SEU Cross Section, cm ²			
LET MeV·cm ² /mg	Conventional	SET Tolerant Global Clock	SET Tolerant Local Clocks
3.4	0.00E+00	0.00E+00	0.00E+00
7.0	0.00E+00	0.00E+00	0.00E+00
11.4	4.04E-08	0.00E+00	0.00E+00
20.0	9.59E-08	0.00E+00	0.00E+00
26.2	1.43E-07	0.00E+00	2.27E-09
35.0	3.39E-07	0.00E+00	1.01E-08
45.0	4.38E-07	0.00E+00	1.81E-08
55.0	5.80E-07	0.00E+00	2.75E-08
82.6	5.15E-07	0.00E+00	3.22E-08
100.0	5.87E-07	0.00E+00	3.81E-08
120.0	6.43E-07	0.00E+00	3.89E-08

- Test structure is 32-bit shift register with no logic blocks
- Testing performed at the Tandem Van de Graaff at Brookhaven National Laboratory
- Results are for 0.35 μ m technology at 3.0V, 32MHz
- Devices that do not upset for LET values of 30 or greater are SEU immune for most practical cases

Experimental Results

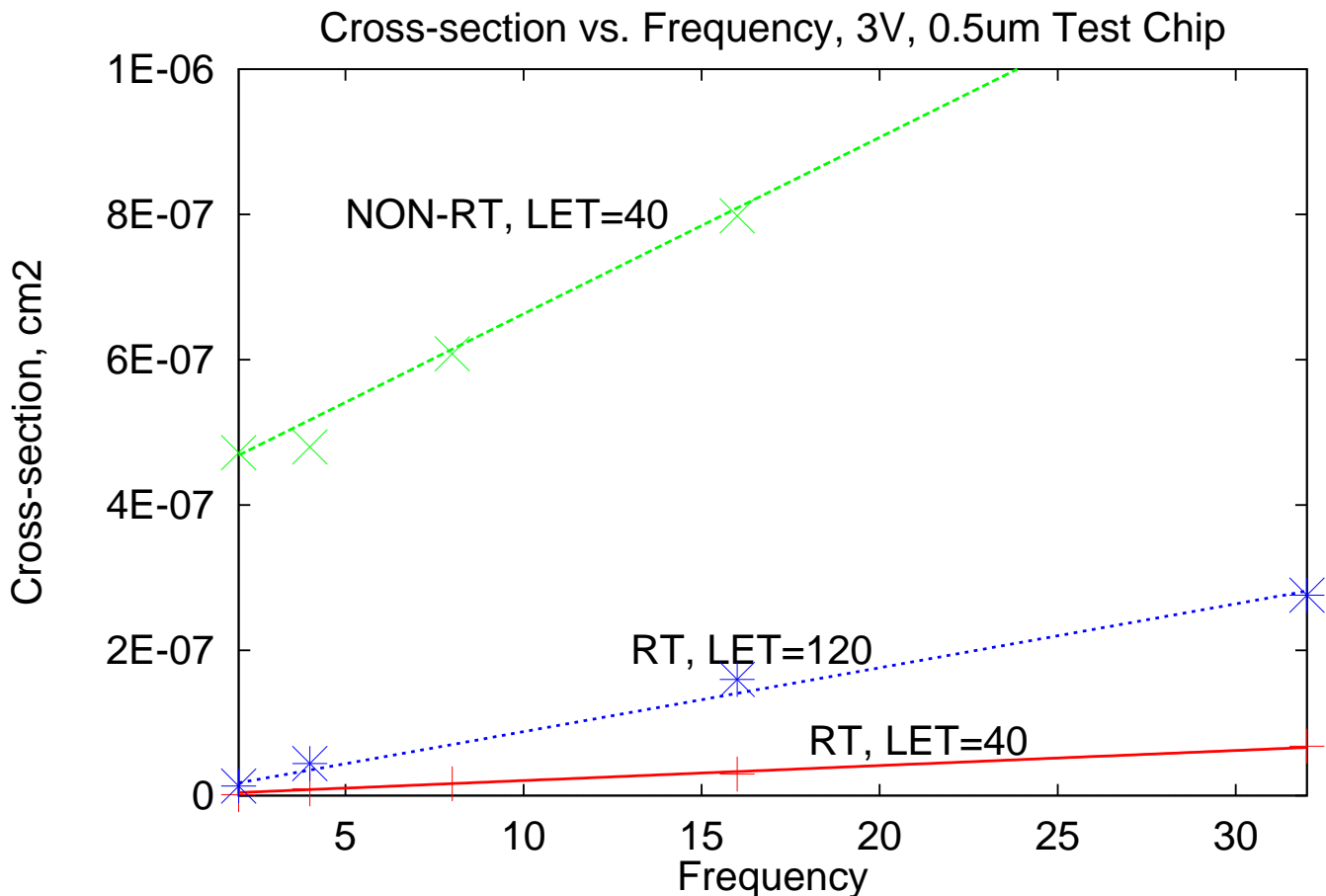
Upsets From SET In Logic



- Test structure is 32-bit shift register with logic blocks between flip-flops
- Results are for 0.35 μ m technology at 3.0V, 32MHz

Experimental Results

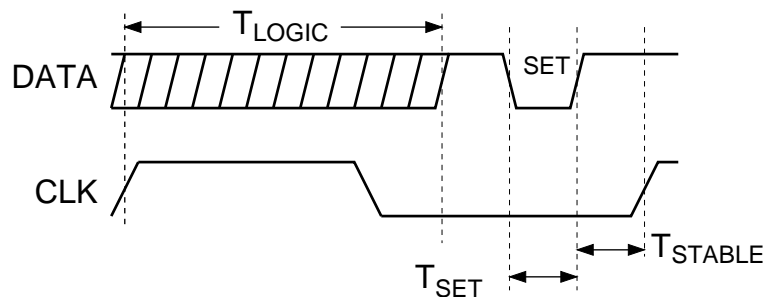
Upset Rate vs. Clock Frequency



- 'RT' is radiation tolerant, 'non-RT' is conventional design
- Results are for 0.5 μ m technology at 3.0V, 32MHz

Design Considerations

- Start with SEU immune flip-flops
- Harden clock signals and asynchronous resets
- Enforce minimum recovery time
- Optimize gates to minimize pulse spreading
- Increase effective setup time



- Test at high clock frequency!