Single Event Transients in Deep Submicron CMOS

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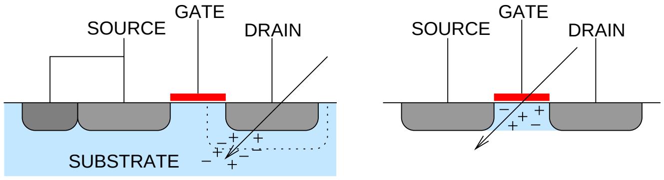
Abstract—**Single Event Transients (SET) occur when an energetic subatomic particle strikes a combinational logic element. The charge deposited by the particle causes a transient voltage disturbance, which can propagate to a storage element and be latched, resulting in Single Event Upset (SEU). The logic design style, storage element behavior, and system timing requirements greatly impact the probability that an SET will cause an SEU. These effects are explored through circuit simulations and heavy ion testing of prototype devices.**

I. Introduction

Single Event Effects occur when an energetic subatomic particle passes through an electronic device. These particles are common in the natural space environment, ranging from neutrons and protons to large atomic nuclei (cosmic particles). In terrestrial applications the particles typically originate in the normal radioactive decay of integrated circuit packaging materials or are created by interactions between cosmic neutrons and atoms in the atmosphere. The particle strikes atoms in the silicon lattice, causing hole-electron pairs to be produced (Figure 1). In bulk CMOS the most sensitive areas are depletion regions at transistor drains. Hole-electron pairs produced here will be swept apart by the electric field such that the injected charge tends to change the state of the struck node with a brief voltage pulse. Silicon-on-insulator transistors also suffer from a different effect, where hole-electron pairs injected into the transistor body may trigger a bipolar action, resulting in current flow that is even greater than the injected current.

Researchers have traditionally focused on the problems of Single Event Upset (SEU) and Single Event Latchup (SEL). SEU occurs when a cosmic particle strikes a transistor inside a flip-flop or memory bit cell. The injected charge produces a voltage disturbance that can cause the storage element to change state. SEL occurs when the injected charge activates the parasitic PNPN structure that exists in bulk CMOS transistors. SEL is not a threat to SOI devices and can be prevented in bulk CMOS by using thin epitaxial layers or guard rings.

There are two common techniques for avoiding SEU by creating SEU-hardened storage elements. First, high value polysilicon resistors can be added inside the storage elements to slow their write time, acting as a simple RC filter to absorb the undesired voltage pulse [1]. Second, unique circuit configurations (design hardening) can be used to provide information redundancy within the storage element and allow it to recover from a single event [2]–[4]. Resistor hardening requires special processing steps that are not commonly available in commercial manufacturing but uses fewer transistors in the memory cell. Design hardening can be applied to leading-edge commercial processes, somewhat mitigating the larger cell size penalty. Both of the these techniques have been applied to integrated circuits that are being successfully used on spacecraft.



BULK CMOS

SOI CMOS

Fig. 1. Particle Strike to CMOS Transistors

Another effect that has become increasingly important is the Single Event Transient (SET). These transients result when a cosmic particle strikes a sensitive node within combinational logic. A voltage disturbance is produced at that node which may propagate through the logic [5]. The most serious consequences will occur if the disturbance propagates to the clock or asynchronous reset input of a number of flip-flops, causing them all to load incorrect data. On the other hand, if the disturbance propagates to the data input of a flip-flop during the critical setup time then the disturbance may be latched, giving the same net effect as a true SEU [6]–[8]. Although such an event seems unlikely, the vast number of sensitive nodes in a typical circuit results in a significant probability of an upset.

This threat has become increasingly relevant as radiation tolerant systems follow the commercial trend to smaller transistor dimensions and lower supply voltages. In deep submicron technologies the capacitance associated with individual circuit nodes is very small, and large voltage disturbances can be produced from relatively small amounts of deposited charge. These voltage disturbances tend to rise above the power supply voltage (or fall below ground) until a parasitic drain-to-body diode is forward biased, so the voltage swing of a cosmic particle strike is greater than the supply voltage by about one

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diode drop. In older 5-volt devices the voltage disturbance was only about 14% greater than the normal voltage swing of the node, but in 3.3-volt devices the disturbance is 21% larger than a normal voltage swing and the transistors that must restore the correct state of the node will require more time to do so. Unfortunately, deep submicron circuits can easily propagate pulses less than a nanosecond wide so the voltage disturbance is much more likely to appear at a flip-flop data input.

II. CIRCUIT SIMULATIONS

A simplified logic cone is shown in Figure 2. The string of gates consists of alternating three-input NAND and three-input NOR gates. A cosmic particle strike is simulated by injecting $3\mathrm{pC}$ in a $1\mathrm{ns}$ rectangular pulse at the inverter output, as shown in Figure 3. Two such events are simulated, one when the inverter output is high, at $15\mathrm{ns}$, and one when the inverter output is low at $35\mathrm{ns}$. Two logic cone variations are simulated. In one case, the “UNOPTIMIZED GATES”, all NMOS transistors have the same width and all PMOS transistors have the same width which might represent a gate array design style. In the second case, the “OPTIMIZED GATES”, the transistor widths are optimized to minimize pulse spreading.

Note that the input rises at about $5\mathrm{ns}$ and that the propagation delay for a rising edge is roughly equal for the optimized and unoptimized gate chains: both outputs rise at about $10\mathrm{ns}$. A falling edge occurs on the input at about $27\mathrm{ns}$ and the propagation delay through the optimized gates is again approximately $5\mathrm{ns}$. However, the propagation delay through the unoptimized gates is much faster, and this output falls about $3\mathrm{ns}$ after the input falling edge. A falling edge propagates through the unoptimized chain much faster than a rising edge, while the propagation delay for both edge types is roughly equal in the optimized gate chain. Therefore a low pulse will be stretched by about $2\mathrm{ns}$ as it passes through the unoptimized gates, as can be seen in the simulation. Conversely, the width of a high pulse will be reduced and high pulses less than $2\mathrm{ns}$ wide will not propagate to the output at all. The optimized gate chain tends to preserve the pulse width for either polarity since its rising and falling propagation delays are well matched.

The significance of pulse spreading becomes apparent when we consider what might happen if these pulses were to appear at the data input of a flip-flop near the active clock edge. In general, SEU-hardened flip-flops are able to completely ignore narrow voltage pulses at their data input, but for wider pulses the cost of providing this immunity becomes very high. In other words, it is far easier to reject narrow pulses of either polarity than to reject wide pulses of only one polarity.

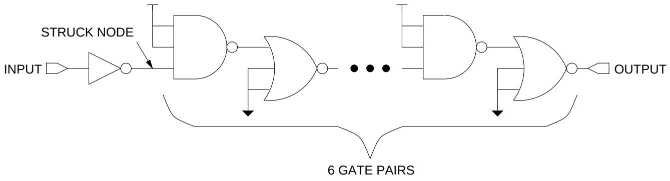

Fig. 2. SET Test Logic

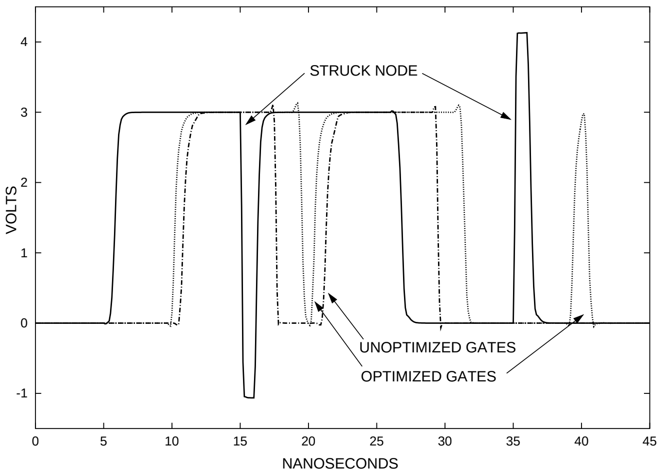

Fig. 3. Simulated Response of SET Test Logic

III. EXPERIMENTAL RESULTS

Test chips designed to characterize these phenomena were manufactured in both $0.5\mu\mathrm{m}$ and $0.35\mu\mathrm{m}$ CMOS processes. The basic test structure was a 32-bit shift register, with a number of variations [9]. Some shift registers had no logic in between the flip-flops while others had a logic cone similar to the one in Figure 2 at the data input of each flip-flop. Some of the logic cones use unoptimized gates while others used optimized gates. In all cases the first stage inverters in the logic cones were designed to be very weak, and their transistor drain areas were enlarged to act as targets for the energetic particles. Data from three different flip-flop circuits was collected, including a conventional, non-radiation-tolerant, flip-flop and two versions of a design-hardened flip-flop. Both of the design hardened flip-flop designs were immune to SEU from particle strikes to the flip-flop itself, but one had also been augmented with circuitry that allowed it to ignore relatively wide transient pulses at the data input.

Cosmic particle strikes were simulated using a heavy ion beam at the Twin Tandem Van de Graaff accelerator at Brookhaven National Laboratory. The Brookhaven facility can produce ion beams of various species to simulate cosmic particles with a broad range of Linear Energy Transfer (LET) levels. The LET of a particle is a measure of how much energy is deposited as it passes through some material. In the natural environment of space the probability distribution of energetic particles falls very rapidly with increasing LET, with the largest population having an LET of $20\ \mathrm{MeV\ cm^2/mg}$ or less. Particles with LET values above about $30\ \mathrm{MeV\ cm^2/mg}$ are exceedingly rare, so a device that does not experience upsets below this value is SEU immune for all practical purposes.

In order to observe the effects of particle strikes in com-

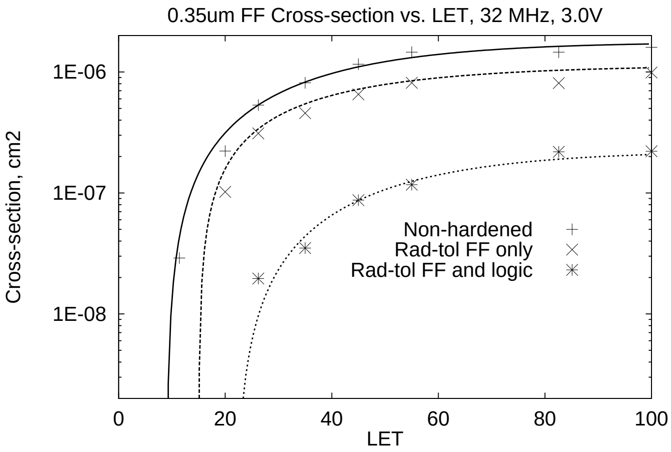

Fig. 4. Heavy Ion Test Data

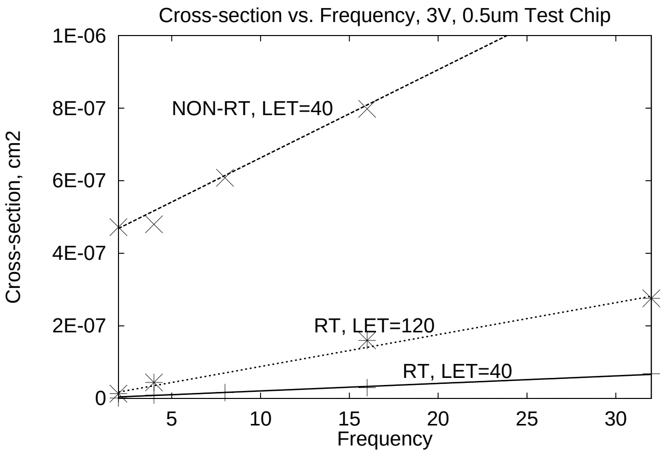

Fig. 5. Upset Cross Section as a Function of Frequency

binational logic the circuits were tested while being clocked at $32\ \mathrm{MHz}$. The measured upset cross section per flip-flop as a function of ion LET for three of the $0.35\mu\mathrm{m}$ shift registers with logic cones is shown in Figure 4. Four sample parts were tested and each was exposed to a total fluence of 1×10^7particles$/\mathrm{cm}^2$. The total number of upsets observed is divided by the total fluence to estimate the sensitive area. The lowest LET value that causes upsets (by striking the most sensitive nodes) is the "LET upset threshold". At high LET levels the particles have sufficient energy to cause an upset when they strike any sensitive node, and this total sensitive area is known as the "saturation cross section". For radiation tolerant design it is desirable to raise the LET upset threshold as high as possible and to minimize the saturation cross section.

The upper curve on the graph indicates the errors for a shift register that uses conventional flip-flops with unoptimized logic cones. These flip-flops have an inherent SEU cross section (without a logic cone) of about $6 \times 10^{-7}\mathrm{cm}^2$ for LET values above $55\ \mathrm{MeV\ cm}^2/\mathrm{mg}$. The same flip-flops in a shift register with unoptimized logic cones have about twice the cross section area, indicating that about half of the upsets are originating in the logic. The middle curve is for a shift register using flip-flops that are immune to SEU from particle strikes within the flip-flop itself with unoptimized logic cones, and in this case *all* of the upsets originate in the logic cone. This curve represents the traditional approach to SEU-immune design, which focuses on the flip-flops but does not deal with transients in the combinational logic. Note that this approach is only marginally better than a conventional non-radiation-tolerant design.

The lowest curve is also for a shift register of SEU-immune flip-flops with logic cones, but in this case the logic gates have been optimized to reduce pulse spreading and the flip-flop circuit was designed to reject narrow pulses on the data input. These optimizations have significantly reduced the saturation cross section and increased the LET upset threshold. Since the probability of a particle strike in the space environment decreases dramatically with increasing LET this represents a substantial improvement. However, it is important to remember that these test structures were designed to explore the behavior of SET, and a functional circuit will most likely have a higher upset threshold and a lower saturation cross section.

The test data also reveal the linear relationship between the upset cross section and shift register clock frequency when logic cones are present, as shown in Figure 5. The figure shows data from $0.5\mu\mathrm{m}$ test structures, but the behavior of the $0.35\mu\mathrm{m}$ shift registers was very similar. This result seems intuitive, because at higher clock frequencies the SET voltage disturbance is more likely to appear at the flip-flop's data input during the critical period near the clock edge. For SEU-immune flip-flops the curve intercepts the cross section axis at zero, which again indicates that all of the upsets seen in these registers originate in the logic cone: if the flip-flop is not clocked, the SET cannot result in an SEU. For conventional flip-flops the curve intercepts the cross section axis at a value roughly equal to the flip-flop's inherent upset cross section. From this data we can conclude that the SEU cross-section of a circuit should be specified as a function of clock frequency, and that the common practice of testing at low clock frequency may grossly underestimate the true vulnerability.

IV. DESIGN CONSIDERATIONS

Traditional approaches to SEU-hardened circuit design rely on flip-flops that are immune to upset from particle strikes to the internal nodes of the flip-flop, and this is still the most important issue. Designing digital systems that also have improved immunity to SET begins by selecting a flip-flop circuit that will ignore transient pulses on the data input and optimizing the logic gates to minimize pulse spreading. There are also several aspects of the design methodology that can impact the final radiation tolerance of the design.

As mentioned earlier, clock signals and asynchronous set/reset signals must be impervious to SET. If the capacitance

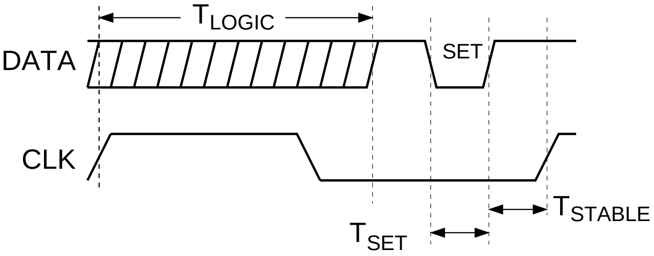

Fig. 6. Effective Setup Time

of these signals is sufficiently high then they can be considered SET immune without additional effort. As a simple rule of thumb, the maximum charge collected during a single event is about $3\ \mathrm{pC}$ for CMOS devices on an epitaxial layer [10]. For example, if the global clock signal has a capacitance of $4\ \mathrm{pF}$ and receives a charge of $3\ \mathrm{pC}$ the largest voltage disturbance possible on that node is $3/4\ \mathrm{V}$. With a power supply voltage of $5\ \mathrm{V}$ this disturbance is unlikely to cause false clocking in a flip-flop, but at a supply voltage of $1.8\ \mathrm{V}$ the same pulse might have disastrous consequences.

The strength of the transistors driving these clock and reset signals is also a factor, as large transistors can drain the single event charge as quickly as it is deposited. This has been a traditional approach to the design of logic circuits that must be SET immune but do not have large nodal capacitance, such as clock phase generators and reset circuits [11]. Unfortunately, it is more difficult to evaluate this characteristic of a circuit. The designer can only estimate the shape and peak value of the current pulse, and several different models are commonly used [2], [12], [13]. For those gates embedded in combinational logic blocks an important consideration is each gate's ability to recover from an SET. Excessive loading or inadequate drive will cause wide SET voltage disturbances.

Providing SET immunity also impacts the effective setup time of flip-flops and this must be taken into account when determining the maximum clock rate of the circuit. Suppose that the combinational logic driving the DATA input of a flip-flop has a total propagation delay of T_{LOGIC}, as shown in Figure 6. For SET immunity it is necessary to consider the possibility that a transient disturbance could arrive at the DATA input at some time after T_{LOGIC}. For a flip-flop designed for SET immunity, the input must be in the correct logic state for at least T_{STABLE} before the flip-flop will assume the correct state (a logic '1' in this example). Once this has happened the DATA input can experience transient error pulses where $T_{SET} < T_{STABLE}$ without causing the flip-flop to assume the incorrect (logic '0') state. In the optimal design T_{STABLE} will be just larger than T_{SET}. The worst case situation occurs when the transient occurs exactly halfway between T_{LOGIC} and the clock edge, dividing the effective data setup time in half. In this case DATA must be valid for a period just equal to T_{STABLE}, either before or after the SET pulse (or both). In the worst case situation then the effective setup time of the flip-flop is approximately $T_{EFFECTIVE\ SETUP} = (2 \times T_{STABLE}) + T_{SET}$. In the optimal design the effective setup time becomes $T_{EFFECTIVE\ SETUP} = 3 \times T_{SET}$. In other words, the effective setup time is roughly three times the width of the largest SET pulse that can appear at the DATA input.

V. CONCLUSION

Single event transients can cause upsets in flip-flops when they propagate to the flip-flop data input near the clock edge. The threat of such upsets has become more significant as radiation-tolerant systems begin to incorporate deep submicron CMOS devices. If ignored, these upsets may erase the benefit of using SEU-immune flip-flops, and testing at low clock frequencies can hide the severity of this problem. Techniques have been developed to mitigate the effect of SET. These techniques were incorporated into test circuits and demonstrated a significant improvement with heavy ion testing.

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